New Trends of Nonlinear Modeling for Microwave Devices in a Circuit/System Environment.

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ABSTRACT : *Specific pulsed measurement techniques are presented to discriminate thermal and trapping effects during the modeling process. An electrothermal modeling approach, a new trap model and a specific nonlinear distributed topology are proposed. Moreover, a new time domain load-pull set-up has been developed to aid in the nonlinear model validation under one and two-tone excitations.*

INTRODUCTION

The availability of reliable nonlinear models for active devices is one of the major challenge for the CAD of microwave circuits. It has implied the development of new pulsed measurement techniques in order to overcome the problems related to specific behaviors of devices such as self heating, distributed effects encountered at high frequencies and frequency dispersion due to traps. Moreover, the accuracy of the models has to be checked so that they provide reliable results when implemented into CAD software. For power applications, the validation procedure is essentially based on load-pull measurements in the frequency domain and newly in the time domain (1). The aim of this paper is to present an overview of up-to-date pulsed measurement techniques taking account of thermal, trapping and distributed effects.

NONLINEAR MODELING BASED ON PULSED MEASUREMENTS

When performing DC measurements, it is not possible to separate temperature and trap influences from those of the other controlling variables in the transistor since self heating and trapping effects modify the device behavior when the control voltages are changed. However, it has been shown that an accurate device characterization must be made under pulsed bias conditions for both I-V and S-parameter measurements (2,3).

Short instantanenous pulses arising from a quiescent bias level are simultaneously applied to the device ports so that I-V characteristics are measured during the pulses. Moreover, a pulsed vectorial network analyzer (VNA) switches on the RF supply to simultaneously superimpose a low level RF stimulus on the instantaneous bias pulse so that pulsed S-parameters may be measured during a short time window. If we ensure that the pulse duration and period are respectively shorter and longer than the thermal time constant, the thermal state of the device is fully controlled by the quiescent level of the bias voltage. In the particular case of FETs, trapping effects can be discriminated by applying pulses from different quiescent levels placed on a dissipated power hyperbola (isothermal) of the I-V characteristics.

An integrated pulsed set-up has been developed in our laboratory. It includes voltage/current probes, a 4-channel digitizing oscilloscope triggered with two pulse generators, a pulsed VNA and a thermal enclosure for electrothermal characterization. The bias tees ensure the connection between the DC and RF parts of the set-up. Pulse duration ranges from 150ns to 1µs depending on the device to be measured and the RF frequency range is 1 to 40GHz. This set-up and the specific pulsed techniques are fully computer controlled (all measurements are made without device disconnection). An open database has been defined providing a direct interface to the modeling activity using different equivalent circuits, analytical model equations, splines or neural networks.

EXTENDING MODEL CAPABILITIES

Thermal Effects : Our thermal modeling approach (4,5) is based on the determination of the RC equivalent thermal circuit relating the instantaneous dissipated power within the device to the actual temperature under large signal excitations. Nonlinear model parameters are expressed by a set of temperature dependent equations so that the ambient temperature and the self heating effects are taken into account by considering the temperature as a new controlling variable of the transistor characteristics. Consequently, a CAD oriented nonlinear electrothermal model is derived and when RF signals are applied, HB simulators solve simultaneously the coupled thermal and electrical equivalent circuits during the convergence loop to dynamically derive the steady-state temperature as a new controlling variable.

The thermal resistance is determined by pulsed measurements of the input diode characteristic using the threshold voltage (V_{BE} or V_{GS}) as an electrical thermometer. First of all for a calibration purpose, the input diode is measured

under pulsed conditions V_{CAL} (V_{BECAL} or V_{GSCAL}) for an imposed constant diode current I_{CAL} at various temperatures T fixed by the thermal enclosure (a quiescent bias level with no dissipated power is imposed). The measured calibration curve $V_{CAL}(T)$ represents the rate of reduction of (V_{BE} or V_{GS}) with T at a constant diode current I_{CAL}. In a second step, the transistor is placed at the ambient temperature T_A and we apply a DC quiescent level to make it dissipate a given DC power P_{DC}. Then, by adding short pulses to reach the previous calibration current I_{CAL}, we do not modify the thermal state controlled by P_{DC} and we measure the new voltage V_{NEW} (V_{BENEW} or V_{GSNEW}). Finally, thanks to the previous calibration curve $V_{CAL}(T)$ (Fig.1), the difference between V_{NEW} and V_{CAL} gives us the temperature rise ΔT above T_A and the thermal resistance is deduced as the ratio of the temperature rise ΔT to the dissipated power P_{DC}.

The thermal capacitance is also derived from specific pulsed measurements through the determination of the thermal time constant. The measurement principle is based on (heating/cooling) pulse cycles applied to the device using a pulse duration much longer than the estimated thermal time constant to heat up the transistor and, a very small recurrence. Under these pulsed conditions, the transistor reaches the equilibrium hot temperature during the long heating pulse but the small recurrence ensure a return to the steady-state cold temperature of the quiescent level. During the heating pulse (~10µs), a specific electrical parameter is chosen to serve as an electrical thermometer. For bipolar transistors, the chosen parameter is the I_C pulse versus time (i.e. temperature) measured on the oscilloscope while for FETs, we measure the decrease of mag(S_{21}) versus time (i.e. temperature) on the pulsed VNA by moving a 100ns RF measurement window along the heating pulse (Fig.2). Finally, given the thermal resistance value previously determined, the thermal capacitance value is adjusted into the thermal circuit by fitting the exponential variation of the electrical thermometer with time (i.e. temperature). Moreover, in the case of FETs, all measurements are performed at a constant V_{DS} voltage in order to ensure that trapping effects do not modify the thermal characterization.

Trapping Effects : GaAs FETs are very sensitive to trapping effects resulting in a frequency dispersion and a strong dependency of their I-V characteristics on the V_{DS} voltage. Our modeling approach (6) is based on the separation of trapping and thermal effects both in the model topology and during the pulsed measurement process. Firstly, we present on Fig.3 the effects of traps on hot pulsed I-V measurements performed with a particular care to avoid thermal effects. The three sets of pulsed I-V curves starting from different V_{DSO} bias points (3, 6 and 9V) are placed on the same dissipated power hyperbola of 250mW. Consequently, the device temperature is identical for the three pulsed I-V curves and the large differences observed between the characteristics are only due to the presence of traps that depends on the quiescent bias point (V_{DSO}, I_{DSO}). According to our experience on extensive pulsed characterizations of many FETs, trapping effects are mainly dependent on the V_{DS} voltage.

We present in Fig.4 the current transients measured on the oscilloscope using a DC bias point and a pulsed point placed on the same dissipated power hyperbola (i.e. at the same temperature) with V_{DS} varying from 1V to 9V. One can observe the capture and emission times of traps. When the drain voltage is high, electrons are captured in ionized deep level traps if the applied pulse duration is longer than the capture time which depends on the electron concentration. As observed in Fig.4, a large part of deep level traps are filled in a few tens of nanoseconds. Consequently, the space charge at the edge of the channel/substrate junction increases leading to a channel thickness reduction and therefore to a decrease of drain current to its steady state. When V_{DS} falls from 9V to 1V, the captured electrons are slowly emitted in a few milliseconds by the deep level traps, the channel thickness slowly increases and the I_{DS} current reaches its steady state value after 4ms. Note that trap capture is very fast compared with trap emission.

It has been shown that trapping effects can be modeled as a self backgating effect (7) : the trap charges are supposed to act as a pseudo-backgate terminal voltage V_B. On Fig.5, we represent the model topology that integrates the trap model in area (a) with the backgate potential V_B. The trap charges are stored in two capacitors C_{BD} and C_{BS} connected between drain and source so that the equivalent complete backgate capacitor is (C_B=C_{BD}+C_{BS}).

For DC values of V_{DS} or at low frequencies, both capture/emission phenomena are achieved so that V_B is proportional to V_{DS} with a coefficient α_R. This proportional relationship is modeled by two series resistors R_{BD} and R_{BS}.

$$\mathbf{R_B} = \frac{\mathbf{R_{BS}}}{\mathbf{R_{BD}} + \mathbf{R_{BS}}} \qquad (1)$$

When RF signals are applied, the capture or emission of traps do not have enough time to occur and the backgate voltage V_B follows the instantaneous C_{BD} charge with a small coefficient α_C.

$$\alpha_C = \frac{\mathbf{C_{BD}}}{\mathbf{C_{BD}} + \mathbf{C_{BS}}} \qquad (2)$$

At intermediate frequencies, V_B reaches a steady state value after a delay that depends on the sign and amplitude of the V_{DS} variation. Our model describes the electron capture and emission with a parallel circuit consisting of a diode D_B and a resistor R_B. The R_B resistor empties the charges in the case of emission while capture is performed through the D_B diode controlled by the backgate potential V_B. As soon as (C_{BD}, C_{BS}, R_{BS} and R_{BD}) are fixed, the R_B and D_B parameters are determined by the capture and emission times derived from the pulsed current transients measured on the oscilloscope. The emission time is supposed constant and expressed by (τ_E=R_B.C_B). For capture phenomenon modeling,

the D_B diode current is :

$$I_{DB} = I_S \cdot \left(\exp\left(\frac{q}{k.T} . \Delta V_B \right) - 1 \right) \tag{3}$$

When V_B varies, the free electron concentration is modified leading to the change of the trap capture time τ_C :

$$\tau_C = R_{DB} . C_B = \frac{k.T}{q.I_{DB}} . C_B \tag{4}$$

In the case of pulsed measurements with 300ns pulse durations, the capture of traps can occur for an instantaneous pulse level V_{DSI} higher than V_{DSO} while in the case of a pulse level V_{DSI} lower than V_{DSO}, the pulse duration is too short to allow the emission phenomena to begin. Therefore, the backgate voltage is calculated with the following equations in order to fit the measured pulsed I-V curves.

$$V_B = \begin{cases} \alpha_R . V_{DSO} & \text{if } V_{DSi} < V_{DSO} \\ \alpha_R . V_{DSO} + \alpha_C .(V_{DSi} - V_{DSO}) & \text{if } V_{DSi} > V_{DSO} \end{cases} \tag{5}$$

The key point of our approach for trap phenomenon modeling is to modify the V_{GS} control voltage of the drain current source I_{DS} by including the backgate voltage V_B in the expression of the new control voltage $V_{GS\text{-}B}$ of I_{DS}:

$$V_{GS-B} = V_{GS} - \alpha_B . V_B \tag{6}$$

Using the expressions of V_B and $V_{GS\text{-}B}$, the three static parameters α_B, α_C and α_R are simultaneously optimized with the drain current model parameters. Note that this method takes account of trapping effects on the drain current so that it can be easily implemented in many kinds of drain current models.

DC and RF control voltages are not separated in our modeling approach in order to integrate dynamical behavior of the model versus biasing, heating and also capture/emission of charges. This dynamical behavior of trapping and thermal effects is a key point for the prediction of slowly-varying envelope modulations and, the computation of self-biasing and self-heating effects versus RF signals.

Distributed Effects : The classical FET model based on a simple π topology is not able to reproduce the distributed nature of the device influencing power saturation at high frequencies, intermodulation and nonlinear noise behavior. To address these problems, we have developed a new FET model (8) based on a double π topology (Fig.6) integrating an internal node. The key point of our approach is to consider the region under the gate as an active transmission line (9). The double π topology is the simplest distributed one reaching a compromise between an electrical distributed circuit and a direct extraction of its elements from pulsed I-V and pulsed S-parameter measurement data.

Each cell is constituted by a nonlinear voltage-controlled current source (I_1, I_2) and its associated time delay (τ_1, τ_2) to take account of the non instantaneous response of both current sources. The distributed gate current is modeled with three diodes (I_{d1}, I_{d2}, I_{d3}) placed in parallel with the capacitances (C_1, C_2, C_3) distributed along the active line. The extrinsic elements have exactly the same topology and values than those used in the classical model and are extracted by a specific method (10). The intrinsic Y-parameter expressions given in (8) allow the extraction of the intrinsic model elements (C_1, C_2, C_3, C_4, τ_1, τ_2) for all bias points since conductances and transconductances (g_{m1}, g_{m2}, g_{d1}, g_{d2}) are previously determined from the measured I-V derivatives of I_1 and I_2. As experienced on many devices, the model parameters (C_2, C_3, C_4, τ_1, τ_2) can be considered as linear elements and fixed to their small signal average value.

The drain current model is made of two current sources controlled by four different voltages. The current I_1 (resp. I_2) is controlled by the voltages V_1 and V_{d1} (resp. V_2 and V_{d2}). Both currents are described by the same equation. Differences between I_1 and I_2 are only due to the different biasing conditions of the two cells. Their values are extracted from the pulsed I-V measurements. Note that for an usual operating point (no gate conduction and no breakdown) the drain current is only due to I_1 and I_2 connected in series. Therefore, both sources should provide the same current although their control voltages are different.

The bias dependence of the capacitance C_1 is described with an analytical equation and for the sake of simplicity, only the dependence of C_1 versus its own voltage V_1 has been taken into account in the nonlinear model. In addition, each distributed diode (I_{d1}, I_{d2}, I_{d3}) is controlled by its own voltage and modeled by a classical exponential equation whose parameters (I_S and α) are chosen identical. Nevertheless, due to the distributed topology, note that the gate current I_{d1} (near the source) is larger than I_{d3} (near the drain) in agreement with the actual physical phenomenon.

The distributed model has been extensively compared with the classical one and its accuracy validated by power and intermodulation measurements. Great improvements in the power saturation behaviors have been obtained at high frequencies of operation due to an earlier compression of the distributed model. The use of a distributed model is of prime importance in the design of millimeter wave circuits above 40GHz. Further investigations are under progress in the field of linearity and noise modeling because the double π topology integrating an internal node provides a new way to model the frequency mixing phenomena and to include the noise sources.

ASSERTING THE MODEL RELIABILITY THROUGH MEASUREMENTS

The accuracy of nonlinear models has to be checked so that they produce reliable results when implemented into CAD software. The model validation process is often the weak point of the proposed models. In a first step, the model should be able to reproduce all the measurements performed for its own extraction but it has also to be consistent with large signal measurements not included in its extraction procedure. For the investigation of power saturation mechanisms, large signal characterizations are essentially based on both frequency and time domain load-pull measurements under one and two-tone excitations.

Validation Between Pulsed I-V and Pulsed S-parameter Measurements : The first validation step is to check at low and high frequencies, the agreement obtained between pulsed I-V derivatives and pulsed S-parameters in the whole working domain of transistors (2) (e.g. in the case of FETs, g_m and g_d derived from pulsed S-parameters are systematically compared with the pulsed I_{DS} derivatives). Measured I-V characteristics and S-parameters are compared with the simulated ones and in the case of electrothermal model validation, DC measurements and simulations of input/output I-V curves are checked.

Frequency and Time Domain/Load-Pull Measurement System : During the last years, measurements of microwave time domain waveforms in a 50Ω environment have been reported. However, we have recently developed a new measurement system (1) which can be viewed as a « time domain load-pull set-up » using our previous set-up dedicated to frequency load-pull measurements. This new system is based on the combination of an harmonic source and load-pull set-up with a modified vector network analyzer. It allows the control and measurement of microwave time domain current/voltage waveforms at both ports of the device with the first three harmonic loads controlled by three independent active loops. The key point of this novel time domain characterization is based on a specific phase calibration (1) to derive the absolute phases of each measured power waves (a_i, b_j) in order to calculate the corresponding time domain current/voltage waveforms.

These new capabilities provide an extensive insight into the operation mode of transistors and a better understanding of their nonlinear behavior at large RF power levels. This new measurement system has been extensively applied to the validation of nonlinear electrothermal models for HBTs and FETs (with trapping effects) under one and two-tone excitations (1). Some validation examples are given in the next subsection.

Further investigations are under progress in nonlinear measurements by monitoring the time domain characterization under pulsed bias conditions for radar applications. Another objective is focussed on the characterization of devices under large signal multitone carriers (NPR set-up) associated to the model validation for circuit and system simulations using circuit envelope simulators (11).

Validation Examples : A 240μm^2 emitter periphery GaInP/GaAs HBT was measured under a single tone 1.8GHz large signal excitation at a class B bias point (V_{BEO}=1V ,V_{CEO}=7V). Load impedances were optimized at the first three harmonics for maximum power added efficiency by tuning the active loops. On Fig.7, one can observe the good agreement obtained for voltage/current waveforms between measurements and simulations using the nonlinear electrothermal model. Moreover, the same device was measured using two-tone excitations ($\Delta f = \pm$ 50kHz) under a non constant envelope microwave signal. The beat period was set to 10μs while the thermal time constant of this device was around 1μs . The Fig.8 shows the measured non constant envelope voltage and current waveforms. Such characteristics recorded under large signal RF levels provide a visual inspection of the distortions for the carrier and the envelope of signals. They also provide information to identify the loci where specific distortions are not well modeled (e.g. linear or saturated regions ; input or output current/voltage).

To investigate the high frequency behavior of the nonlinear electrothermal model associated to its embedding trap model, load-pull measurements have been carried out at 10GHz for several bias points and compared with simulation results in the case of a (400μm x 0.7μm) FET from Thomson foundry. The Fig.9 shows the good agreement obtained between measured and simulated output power and power added efficiency in class AB. At all bias points, the same agreement has been observed for power saturation and efficiency.

CONCLUSION

Nonlinear modeling of active devices still represents a complex task and a major challenge for the success of microwave circuit CAD. It has been shown that specific pulsed measurement techniques of S-parameters and I-V characteristics provide reliable and efficient ways to characterize electrical, trapping, thermal and distributed effects. From these measurements, various electrical model topologies can be extracted depending on the dedicated application. Finally, model verification is performed by both frequency and time domain load-pull measurements.

REFERENCES

(1) D. Barataud, A. Mallet, M. Campovecchio, J.M. Nebus, J.P. Villotte, J. Verspecht ; « Measurements of time domain voltage/current waveforms at RF and microwave frequencies for the characterization of nonlinear devices » : IEEE Instrumentation and Measurement Digest, 1998, pp1006-1010.

(2) J.P. Teyssier, M. Campovecchio, C. Sommet, J. Portilla, R. Quéré ; « A pulsed S-parameter measurement set-up for the nonlinear characterization of FETs and bipolar power transistors » : 23th EuMC Digest, 1993, pp489-494.

(3) J.P. Teyssier, J.P. Viaud, J.J. Raoux, R. Quéré ; « Fully integrated nonlinear modeling and characterization system of microwave transistors with on-wafer pulsed measurements » : IEEE MTT-S Digest, 1995, pp1033-1036.

(4) T. Peyretaillade, M. Perez, S. Mons, R. Sommet, Ph. Auxemery, J.C. Lalaurie, R. Quéré ; « A pulsed measurement based electrothermal model of HBT with thermal stability prediction » : IEEE MTT-S Digest, 1997, pp1515-1518.

(5) M. Campovecchio, R. Sommet, J.P. Teyssier, R. Quéré, J. Obregon ; « Electrothermal modeling of semi-conductor devices for nonlinear microwave and RF CAD » : IEEE MTT-S Symposium ; Workshop on nonlinear CAD, 1997.

(6) Z. Ouarch, J.M. Collantes, J.P. Teyssier, R. Quéré ; « Measurement based nonlinear electrothermal modeling of GaAs FETs with dynamical trapping effects » : IEEE MTT-S Digest, 1998, Baltimore.

(7) K. Kunihiro, Y. Ohno ; « A large-signal equivalent circuit model for substrate-induced drain-lag phenomena in HJFET » : IEEE Trans. on Electron Devices, 1996, Vol. 43, n°9, pp1336-1342.

(8) B. Mallet-Guy, Z. Ouarch, M. Prigent, R. Quéré, J. Obregon ; « A distributed measurement based nonlinear model of FETs for high frequencies applications» : IEEE MTT-S Digest, 1997, pp869-872.

(9) G. Ghione, C. Naldi, F. Filicori ; « Physical modeling of GaAs MESFET in an integrated CAD environment : From device technology to microwave circuit performance » : IEEE Trans. on MTT, 1989, Vol. 37, pp457-468.

(10) J. Portilla, M. Campovecchio, R. Quéré, J. Obregon ; « A new coherent extraction method of FETs and HEMTs models for MMIC applications » : European GaAs Symposium Digest, 1994, Torino.

(11) J. Lajoinie, E. Ngoya, D. Barataud, J.M. Nebus; J. Sombrin, B. Rivierre ; « Efficient simulation of NPR for the optimum design of satellite transponders SSPAs » : IEEE MTT-S Digest, 1998, Baltimore.

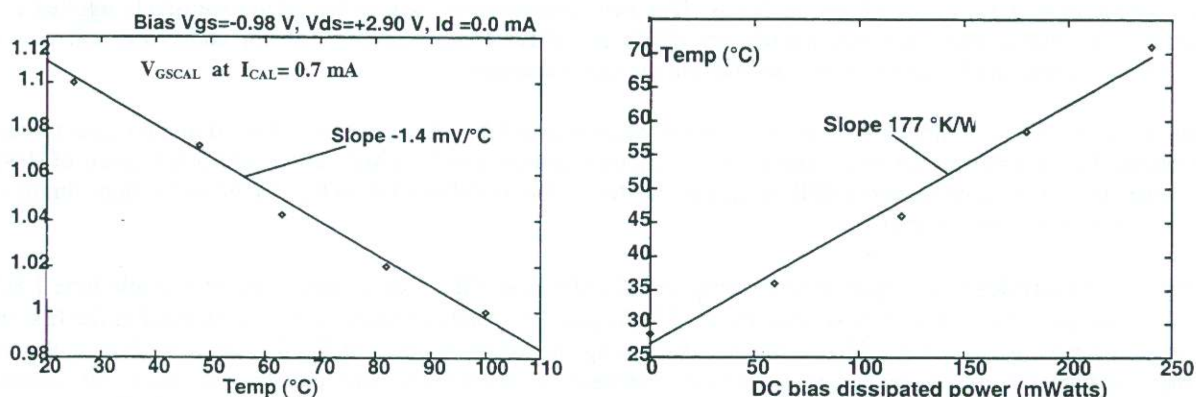

Fig.1 : Pulsed measurement of the input diode and thermal resistance extraction.

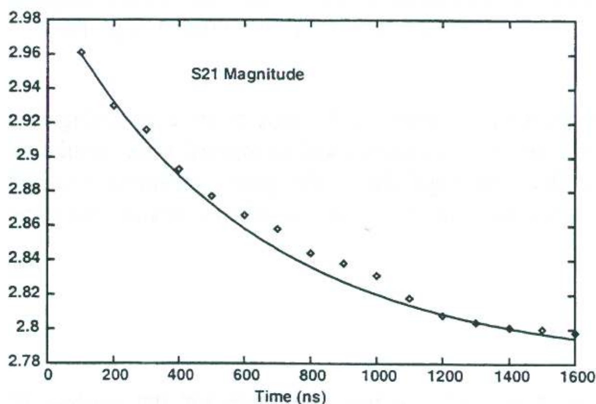

Fig.2 : Pulsed measurement of mag(S_{21}) during the heating pulse for thermal time extraction.

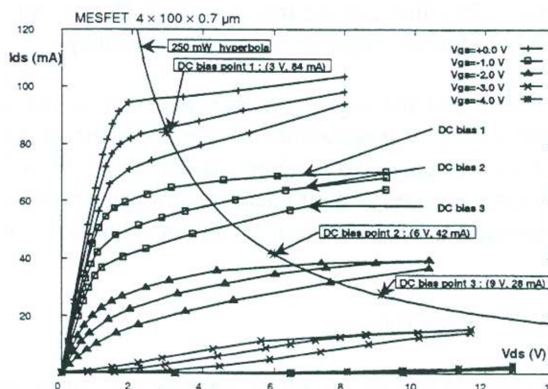

Fig.3 : Pulsed I-V curves at 3 isothermal bias points with P_{DC}=250mW : (3V-84mA) ; (6V-42mA) ; (9V-28mA)

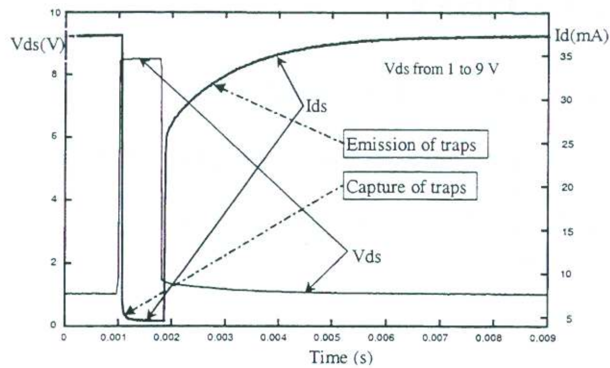

Fig.4 : Voltage/current transients for a pulse applied along the isothermal hyperbola from V_{DS}=1V to 9V.

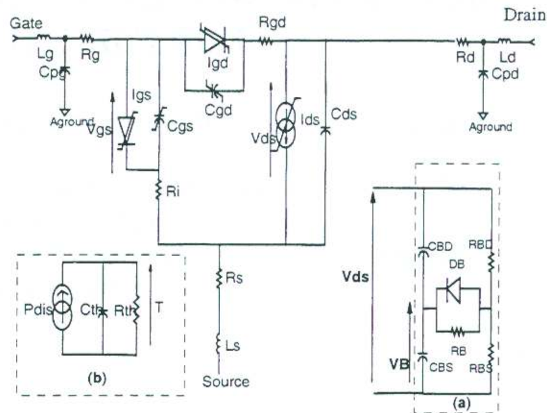

Fig.5 : Nonlinear electrothermal model topology including the embedding trap model in the area (a).

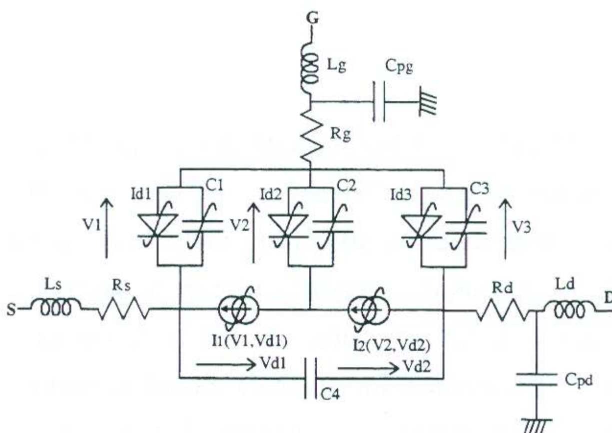

Fig.6 : Nonlinear distributed FET model.

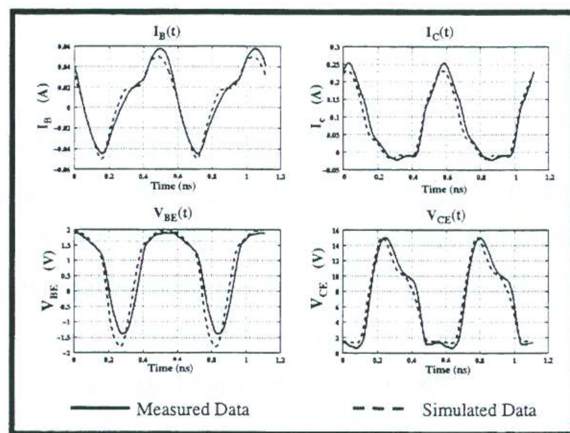

Fig.7 : Measured and simulated voltage/current waveforms in class B at 1.8GHz for a GaInP/GaAs HBT.

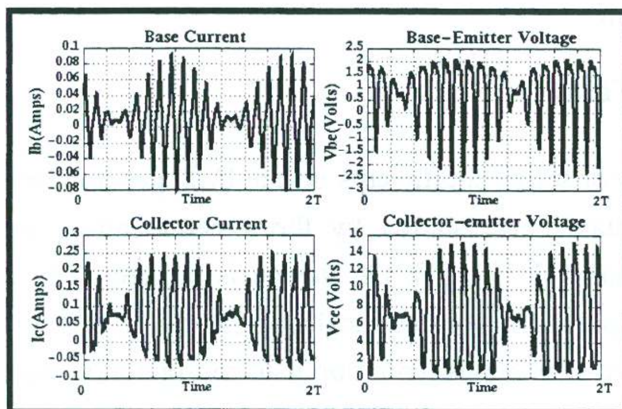

Fig.8 : Measured voltage/current waveforms under 2-tone excitations at 1.8GHz for a GaInP/GaAs HBT.

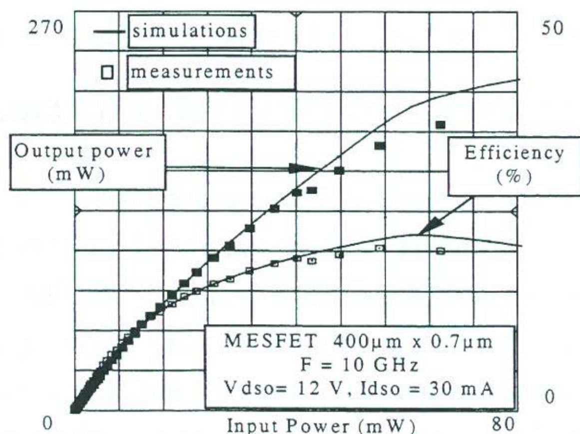

Fig.9 : Measured and simulated output power and PAE at 10GHz in class AB for a 400µm MESFET.