A 23-24 GHz low power frequency synthesizer in 0.25µm SiGe

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***Abstract* — This paper presents the design and the experimental measurements of a 24 GHz fully integrated fractional PLL, for ISM band, with a new low power prescaler. This circuit is implemented in a 0.25 µm SiGe:C process from STMicroelectronics (BiCMOS7RF). The PLL power dissipation is 170 mW and fulfills a 23.7 to 24.9 GHz frequency locking range, while exhibiting a phase noise of -100 dBc/Hz at 100 KHz from the carrier. The simulated PLL unity-gain bandwidth is 36 MHz, with a phase margin of 54°. The PLL uses a new latch-based prescaler (SRO) which exhibits a power dissipation of 0.68 GHz/mW.**

I. INTRODUCTION

Usually in PLL above 20 GHz, an important part of the power dissipation is located in the dividers. Moreover, usually the power dissipation of dividers is very high when the operating frequency is about the half of the NPN transition frequency (FT). For instance, the CML divider-by-16 in [1] achieves 0.37 GHz/mW at 38 GHz, with a NPN FT of 85 GHz.

One way to increase the performances of such CML flip-flop dividers is the inductance peaking. However the silicon area of such dividers is large, due to integrated inductors, and therefore their cost is high. Another way is to use Injection Locked Frequency Dividers or regenerative dividers. However, most of these dividers also use integrated inductors and do not allow dual-modulus division. Furthermore they are often either narrow-band or power hungry. For instance the regenerative divider in [2] achieves 0.07 GHz/mW at 79 GHz with a FT of 80 GHz.

To overcome these limitations, a new latch-based structure was designed to obtain, at the same time, a broadband and a low-power high-frequency divider. This divider provides two division ratios and was used to design a fully integrated fractional PLL at 24 GHz.

II. PLL DESIGN

A. Architecture

In this design, we have chosen to synthesize directly the 24 GHz signal without frequency multiplication. Despite the difficulties of designing the VCO and the prescaler at so high frequencies, we have chosen this solution to achieve a better spectrum purity. The PLL schematic is shown in Fig.1.

The phase detector is a Gilbert cell with a current output. The phase detector output is connected to a passive type II filter. The latter is followed by an active filter for better rejection at higher frequencies. The VCO output attacks the dual-modulus prescaler via a buffer, another buffer supplies the PLL output.

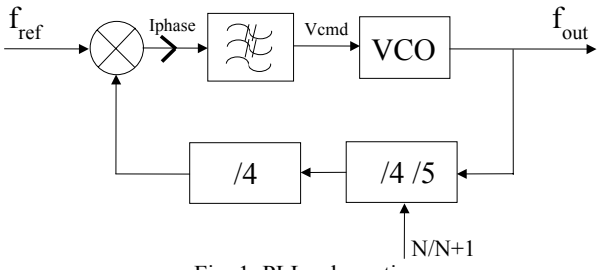

Fig. 1. PLL schematic

The dual-modulus prescaler is realized by a low-power Synchronized Ring Oscillator structure (SRO) described in [3]. Its two division ratios are 4 and 5. The prescaler is followed by an asynchronous divider-by-4. This second stage is realized by two flip-flops in series. In this design, the divider-by-4 and the prescaler are not connected to realize a N/N+1 divider. Indeed, such divider is difficult to design due to timing constraints. We have preferred a simpler and more robust structure without feedback. Therefore, the divider achieves an overall division of 16 or 20.

B. VCO

The VCO is realized by a degenerated cross-coupled bipolar pair loaded by two LC tanks. The VCO schematic is shown in Fig.2. With a FT of 60 GHz, the bipolar transit time is about 2.5 ps. At 24 GHz the dephasing in the VCO loop is above 40°. To compensate this delay, a capacitive degeneration was added to achieve 0° in the oscillator loop at the LC tanks resonance. Without this compensation, the oscillation frequency is below the LC tanks resonance, at a frequency where the LC tanks impedance is lower. So, with this capacitive degeneration the oscillation frequency and amplitude are both increased. A capacitive voltage divider was also placed between the base and the collector of the transistors. It increases the cross-coupled pair linearity and, consequently, maximizes the oscillation amplitude and reduces the phase noise.

The two varactors use matrix of small NMOS transistors. These transistors work in inversion mode. Their geometry was optimized to achieve a good frequency variation (i.e. low parasitic capacitors) with low losses. The VCO command voltage is applied to the drain/source of the transistors, while the gate is wired to the inductors by short connections. The unloaded LC tanks quality factor is about 10. To reduce the VCO sensitivity to substrate noise, the varactors bulk was isolated from the common substrate by a triple-well.

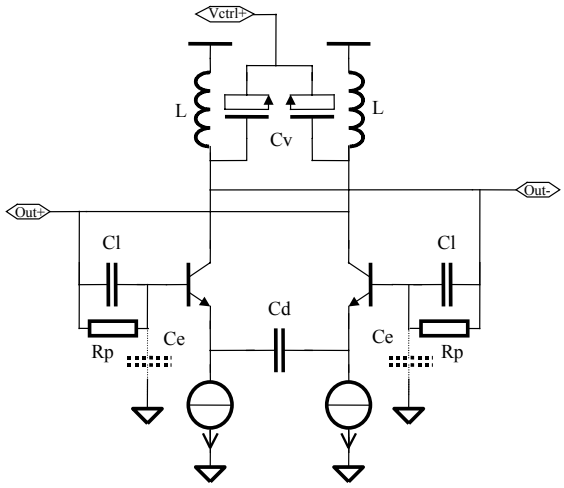

Fig. 2. VCO core schematic

In a previous 24 GHz VCO, the running frequency was measured slightly higher than expected. So in this design, the VCO was designed with a simulated oscillation frequency off by 4%. In simulation the VCO covers 22.3 to 24.0 GHz with a maximum slope of 1.2 GHz/V. The simulated phase noise is -90 dBc/Hz at 100 kHz of the carrier. To achieve a robust oscillation, the biasing current was fixed high. The VCO with its two buffers draws 45 mA, so with a 2.5 V power supply, the total VCO power dissipation is 110 mW.

C. Prescaler

The prescaler is a dual-modulus Synchronized Ring Oscillator divider. This schematic is shown in Fig.3. This divider is similar to the classical 4/5 flip-flop based divider, but with the flip-flop replaced by latches. This new divider uses only the half of latches of the classical 4/5 divider.

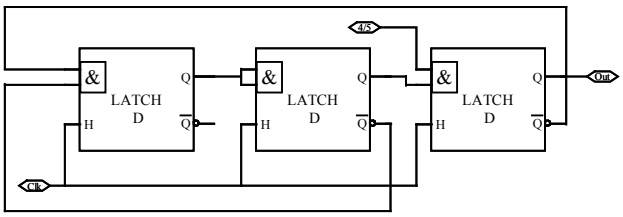

Fig. 3. SRO dual modulus divider schematic

The theoretical behavior study of the SRO divider can be done by viewing the divider like a ring oscillator. The divider latches propagation delay is altered by the clock: when the clock is low, the latches are locked, so the propagation delay is increased until the clock goes high. Therefore, in the synchronization ranges, the latches delay becomes an integer multiple of the clock period. And, like for any ring oscillator, the output period is twice the loop propagation delay. In the principle, the behavior is the same for the flip-flop dividers by 4/5, only the working ranges are different. From this study [3], we found that the efficient (synchronization) ranges are defined by the following double inequality (for 50% clock duty cycle):

$$\frac{n-1/2}{t_p} \le F_{clock} \le \frac{n}{t_p} \quad \text{with n} \in \text{N}^{+*} \qquad (1)$$

where t_p is the propagation delay of the latches (including the AND inputs) when they are transparent, and F_{clock} is the clock frequency. When this condition is fulfilled, the division ratios are:

$$N_1 = 4n \text{ and } N_2 = 5n \text{ with n} \in \text{N}^{+*} \qquad (2)$$

Only the larger solution n=1 is useful. With n=1 the SRO achieves two division ratios of 4 and 5, the theoretical frequency working range is 66% (f_{max}/f_{min}=2). For comparison, the maximum flip-flop based divider is defined by the following inequality:

$$F_{clock} \le \frac{1}{2t_p} \qquad (3)$$

with the same parameters than (1). So (1) and (2) demonstrate that for the same propagation delay (the same power dissipation by latch), the SRO divider achieves twice the maximum operating frequency of the flip-flop divider. Moreover, ideally, with half the number of latches, the power dissipation of this divider is about a quarter of the flip-flop 4/5 divider, all other things being equal. Nevertheless, this lower power dissipation is achieved at the cost of a lower relative frequency working range.

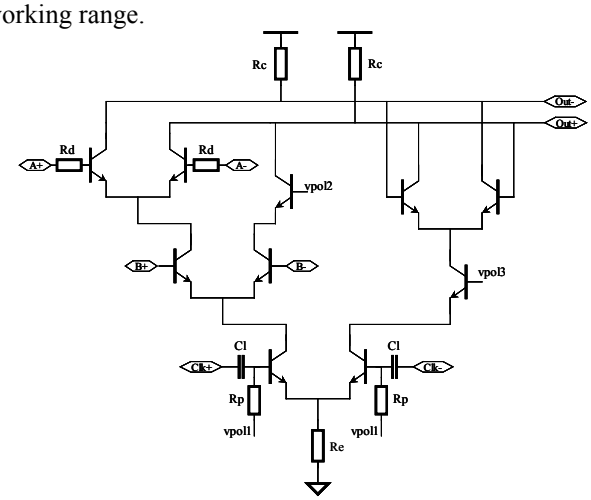

Fig. 4. Dual modulus divider latches schematic

The prescaler is composed of three fully differential latches with AND inputs as depicted in Fig.4. The latches were designed without current source to achieve sufficient voltage headroom for the bipolar transistors. The current source is replaced by a resistor associated with a capacitive coupling of the clock. Emitter followers depicted in Fig.5., realize levels shift for the B inputs. The propagation delay of inputs (A and B) are matched by the addition of two resistors in the A inputs. The

differential outputs swing voltage was set to 500 mV peak to peak.

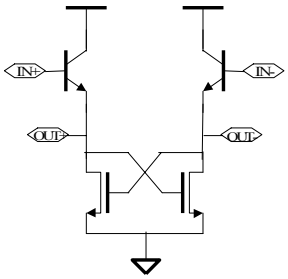

Fig. 5. Levels shifter schematic for B inputs

According to the simulation of division by 4 and 5, the SRO prescaler working range is 19 to 29 GHz. The prescaler draws a current of 13 mA. The overall PLL loop divider (SRO+divider-by-4) draws 17 mA from the 2.5 V power supply. Its simulated output phase noise is -127 dBc/Hz at 100 kHz of the carrier.

D. Loop filter

The first stage of the loop filter is a type II filter shown in Fig.6. This first stage fixes the PLL bandwidth. In simulation, the open loop 0 dB is at 36 MHz, the gain margin is 7 dB and the phase margin is 54°. The 5th order active low-pass filter that follows the passive increases the rejection of high frequencies. This filter removes most of the $2.f_{ref}$ component from the Gilbert cell.

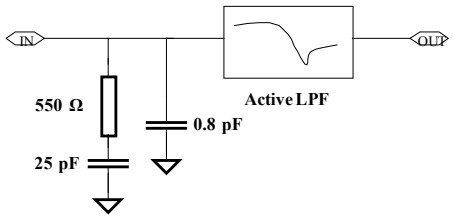

Fig. 6. Loop filter schematic

It is realized by two cells of 2nd and 3rd order in series. These cells are derived from the well-known Sallen and Key filter. The active filter was optimized not to do degrade the phase margin and to provide a high slope after its cut-off frequency. In simulation, its cut-off frequency is 370 MHz, it draws 3 mA from the 2.5 V power supply. Its attenuation is 55 dB above 1 GHz ($\sim f_{ref}$). The simulated locking time of the PLL is about 100 ns.

III. Chip Layout

This PLL was designed in BiCMOS7RF process from STMicroelectronics. This process features 60 GHz SiGe:C HBTs and 0.25 µm CMOS transistors [4]. The process provides high quality passive components: MIM capacitors, high resistive polysilicon resistors and inductors. The microphotograph of the chip is depicted in Fig.7.

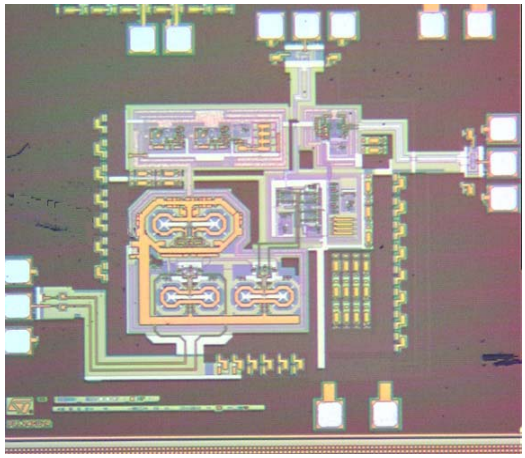

Fig. 7. Chip microphotograph

In the chip, the PLL was integrated together with separated VCO for characterization. Area of the PLL is 1.7 mm² with the pads, the PLL core occupies 0.76 mm² and the prescaler area is 0.025 mm².

VI. Measurements Results

The measurements were realized with high speed probe station, a 26 GHz HP 8563E spectrum analyzer and a 20 GHz HP 83712B signal generator.

The VCO measurements show a frequency range from 23.4 to 25.4 GHz. The VCO slope is 2.7 GHz/V. Its measured power dissipation is 110 mW. As expected, the measured VCO oscillation frequency is 4% higher than the simulated. Its frequency slope is also about twice the simulated one. These differences are caused by the imprecise modeling of varactors at very high frequencies.

The measured free-running VCO phase noise is depicted in Fig.8. The phase noise is -70 dBc/Hz at 100 kHz of the carrier.

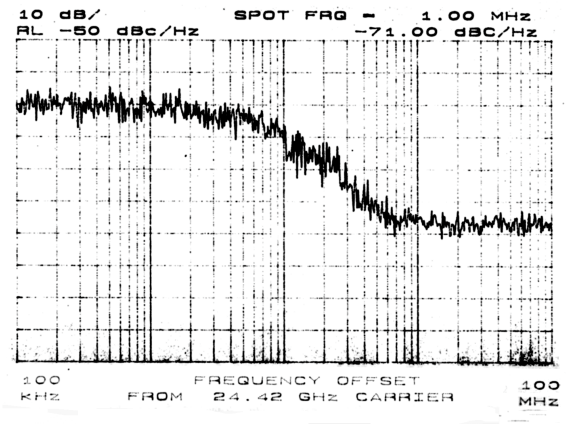

Fig. 8. VCO phase noise at 24.42 GHz

The PLL exhibits a hold frequency range from 23.7 up to 24.9 GHz for N=16 and 23.4 up to 25.16 GHz for N=20. The measured pull-in range is about 100 MHz lower than the hold range. The output spectrum is depicted in Fig.9 for N=20.

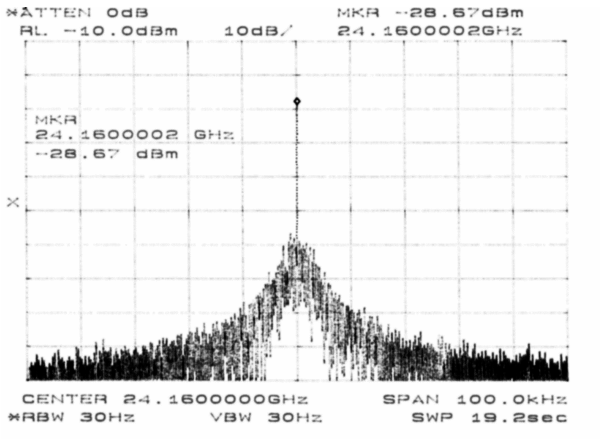

Fig. 9. PLL output spectrum at 24.16 GHz (N=20)

The PLL measured phase noise is -100 dBc/Hz at 100 kHz of the 24.16 GHz carrier for N=16. For N=20, the phase noise is -97 dBc/Hz. Fig.10 shows that the PLL follows the reference phase noise for frequencies up to 100 kHz. According to simulations, above that frequency and up to 10 MHz (PLL bandwidth limit), the first source of phase noise is the divider.

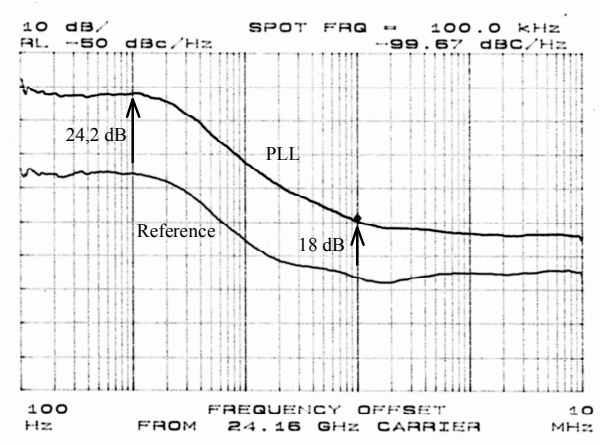

Fig. 10. Output phase noise at 24.16 GHz (N=16)

Below 100 kHz, the shift is 24.2 dB, near the theoretical value of 20.log(16)=24.1 dB. Therefore, the actual PLL phase noise is without doubts far better. The total PLL power dissipation is 170 mW. The overall measured characteristics are reported on Table I.

Technology	ST BiCMOS7RF 0.25µm
PLL	
Frequency range	23.7 - 24.9 GHz
Phase noise N=16	-100 dBc/Hz @ 100 kHz
Phase noise N=20	-97 dBc/Hz @ 100 kHz
Power dissipation	170 mW
PRESCALER	
Frequency range	19 to 29 GHz
Power dissipation (simulation)	43 mW
VCO	
Frequency range	23.4 - 25.4 GHz
Power dissipation	110 mW

TABLE I:
SUMMARY OF MEASURED PLL,VCO AND PRESCALER CHARACTERISTICS

With 0.68 GHz/mW, the SRO prescaler power dissipation is about 1.8 times lower than the best published SiGe divider in Table II.

SIGE PRESCALERS			
	GHz/mW	N	NPN transistors
This work	0.68 @ 29 GHz	16-20	60 GHz - 0.4 µm
[1]	0.37 @ 38 GHz	16	85 GHz - 0.4 µm
[2]	0.07 @ 79 GHz	2	80 GHz - 0.25 µm
[5]	0.35 @ 36 GHz	256-257	85 GHz - 0.2 µm
[6]	0.16 @ 51 GHz	2	120 GHz - ??

TABLE II: COMPARISON TABLE

V. CONCLUSION

A low-power fully-integrated fractional PLL at 24 GHz, with a new low-power latch-based prescaler, was presented in this paper. The PLL measured frequency range is from 23.7 to 24.9 GHz with a power dissipation of 170 mW. This new dual-modulus prescaler is compact (inductor-less), uses only logic blocs and its power dissipation is low. It achieves 0.68 GHz/mW near $F_T/2$ that is superior to other published similar low-power dividers.

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