A 26-40 GHz On Wafer Intermodulation Measurement System

F. Bué, C. Gaquière, Y. Crosnier, B. Carnez*, P. Quentin*

Institut d'Electronique et de Microélectronique du Nord - U.M.R. - C.N.R.S. 9929
Département Hyperfréquence et Semiconducteurs
Cité Scientifique - Avenue Poincaré - B.P. 69 - 59652 Villeneuve d'Ascq cedex – France

* United Monolithic Semiconductors
Route départementale 128 - BP 46 - 91401 Orsay cedex – France

Abstract **— In this paper, a 26 – 40 GHz intermodulation measurement system is presented which permits intermodulation investigations together with load-pull measurements. The one-tone and two-tone responses of Ka PHEMT devices are compared. Inter Modulation Ratio (IMR) optimizations performed by adjusting the output load and bias settings show that it is possible to improve the IMR up to 5-6 dB at a constant output power level.**

I. INTRODUCTION

The microwave telecommunication applications explosion requires the study of HFET devices in power and linearity mode. Due to the carriers proximity it is necessary for these devices to deliver high power density but also to have a linear behaviour. This paper describes an intermodulation measurement system in Ka band. Measurement results are presented which show the possibilities to optimize the IMR versus the bias and output load.

II. MEASUREMENT SYSTEM

A block diagram of the test system is shown in figure 1.

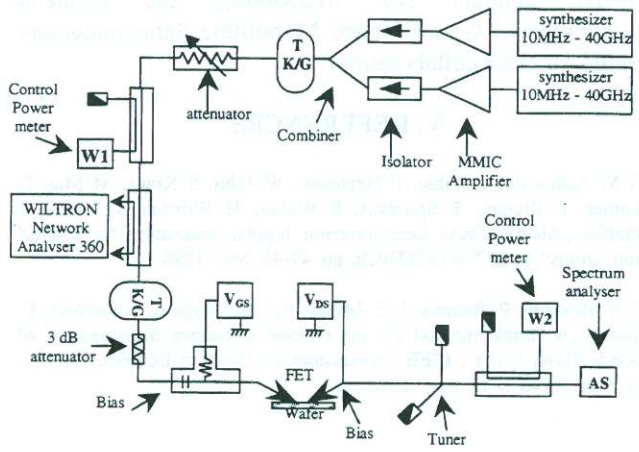

Figure 1 – intermodulation measurement system

Two MMIC's made by UMS are used to amplify separately the excitation frequencies generated by the synthesizers. They are mounted in specific cells and deliver a maximum output power level of 25 dBm at 26GHz. A vector network analyzer measures the input reflection coefficient and the load reflection coefficient of the DUT. A power meter is used to measure the power injected into the transistor. The output load is fixed by the tuner. A power meter and a spectrum analyzer are used to measure the power absorbed by the load and display the third order intermodulation level respectively. Two multimeters provide drain and gate currents measurements.

A special output probe has been developed (coplanar-guide WR28) which allows low loss between the DUT and the tuner (0.7 dB) and in these conditions enables us to match the transistor as well as possible.

The calibration procedure is achieved in two parts. Firstly, a one port calibration is achieved in the input plane of the DUT. The load impedance presented at the output of the device is measured by replacing the DUT by a coplanar line. Secondly, a power calibration is realized, as described in a previous paper [1].

III. EXPERIMENTAL RESULTS

This section presents the experimental results obtained with a double delta doped PHEMT ($2x75x0.25\mu m^2$) realized by UMS. Thanks to an optimized topology (double recess), this device exhibits a current density of 500mA/mm with high breakdown voltages (12V) in diode configuration and in transistor configuration, even at open channel. This allows us to perform power measurements with drain source bias condition up to 8V at open channel without gate current limitation. In all the paper the operating frequency is 26GHz and the two-tone measurements are carried out with a 1MHz spacing.

The figure 2 shows the output power as a function of the input power under single tone excitation with the load impedance optimized for maximum output power

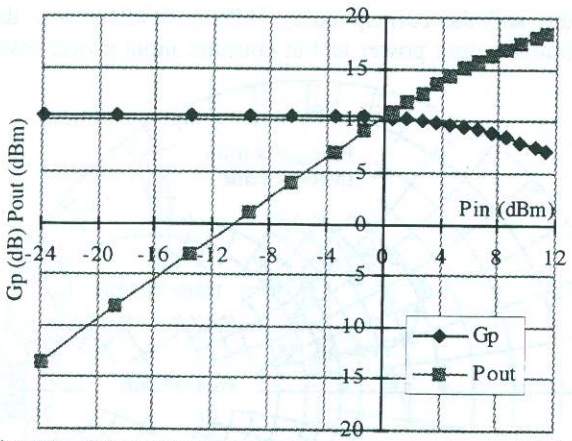

Figure 2 – Output power and power gain versus input power level for the one-tone mode (Vds=5V Id=40% Idmax)

(maximum output power density of 500mW/mm). Then the same device has been studied with a two-tone excitation. Output power for each tones and the third and fifth order intermodulations are shown in figure 3 versus the total input power level for the same optimal load impedance. It is to be noted that the optimal load impedance for power application is the same whatever the excitation mode (one-tone or two-tone).

The third order intermodulation power variation versus input power level shows a slope of 3 at low power level, in good agreement with the theory. When the input power increases the slope falls down like LDMOS [2] . Then, the slope increases strongly before to reach the classical compression of the 3rd IM at high input power level. This behaviour has been noted only for double recess topologies. Indeed, up to now, for single recess topologies,

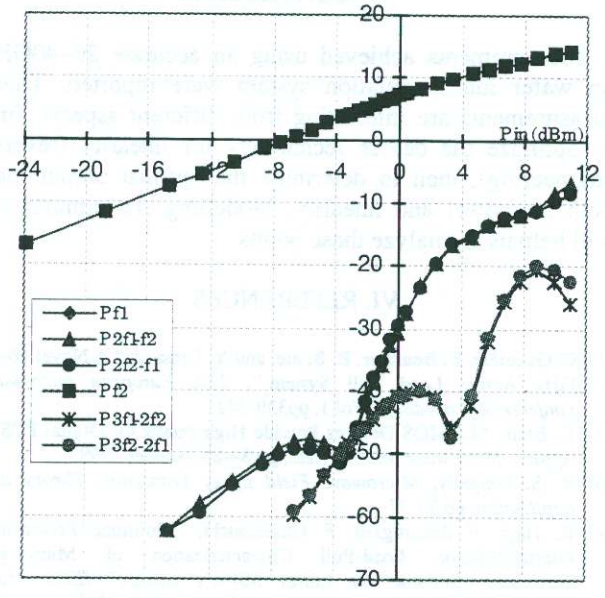

Figure 3 – Output power for each tone and output power for 3rd and 5th IM versus total input power level for two-tone excitation (Vds=5V Id=40%Idmax)

such drop has never been observed. Slope of three are always obtained excepted at high level where the compression effect appears. An attempt of explanation may be the sign of the fifth order coefficient which, at high power level, may influence the slope. Hence, if the transconductance expression is assumed to depend on the input voltage V as follow:

$$Gm(V)=gm_1+gm_2V+gm_3V^2+gm_4V^3+gm_5V^4+gm_6V^5+\ldots$$

$$V=A.\cos\omega_1 t+B.\cos\omega_2 t$$

The magnitude of the drain current at $2f_1-f_2$ is :

$$Id=0.25gm_3A^2B+0.25.gm_5A^4B+0.375gm_5A^2B^3$$

Consequently, if the coefficients gm_3 and gm_5 have different signs, the slope could change [3].

A decrease of the maximum output power has been obtained between the one-tone and the two-tone modes. This behaviour has been already noted at lower frequencies [4]. It is related to the instantaneous amplitude variation due to an AM-like modulation. Indeed, for a same total input power level, the clipping occurs earlier in the two-tone mode than in the one-tone mode (figure 4).

IV. EFFECTS OF BIAS AND LOAD ON THE IMR

Figure 5 shows the IMR levels obtained at a constant output power level and at 1dB compression as a function of the drain-source bias voltage. For each measurement, the device is loaded with the optimal load impedance for maximum output power. When the drain-source bias increases, an improvement of the IMR is established. This behaviour is in close correlation with the forward gate current behaviour. The same study has been carried out

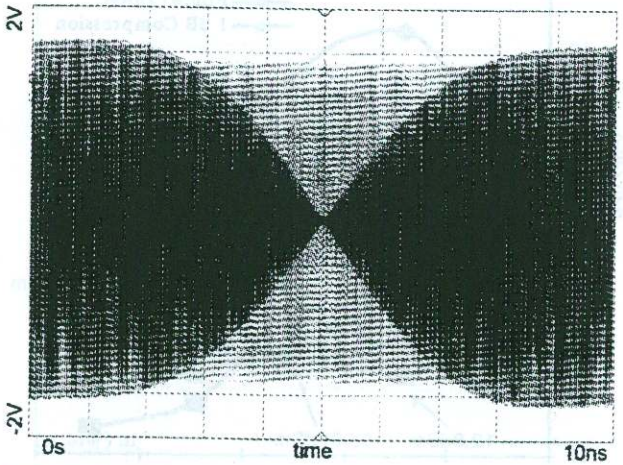

Figure 4 – Output signal variation versus time for one-tone (gray) and two-tone (black) modes at the same total input power level (non linear simulation)

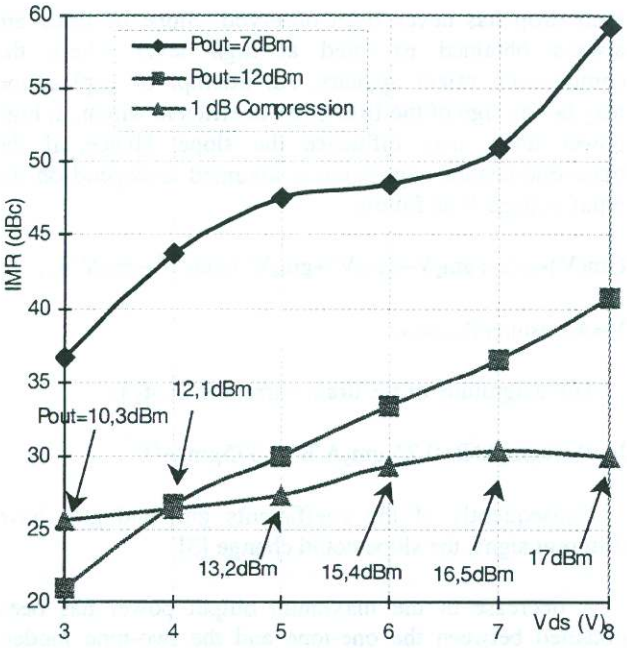

Figure 5 – IMR versus Vds for Pout=7dBm, Pout=12dBm, and Pout=1dB power compression. (Id=40%Idmax)

versus the drain current at a constant drain-source voltage of 5V (figure 6). It can also be observed that, at low input power level, the optimal IMR is obtained near class A operation (50% Id_{max}). Around this point, toward the clipping of gate forward conduction and pinch-off, the IMR is degraded. Under large-signal operating mode (near/or in the compression region), the IMR experiences an increasing degradation with increasing drain current and tends to keep a constant value at high I_{ds}. This type of evolution has already been noted by Ghannouchi [4] but at lower frequency (4GHz).

Then a typical example of constant output power

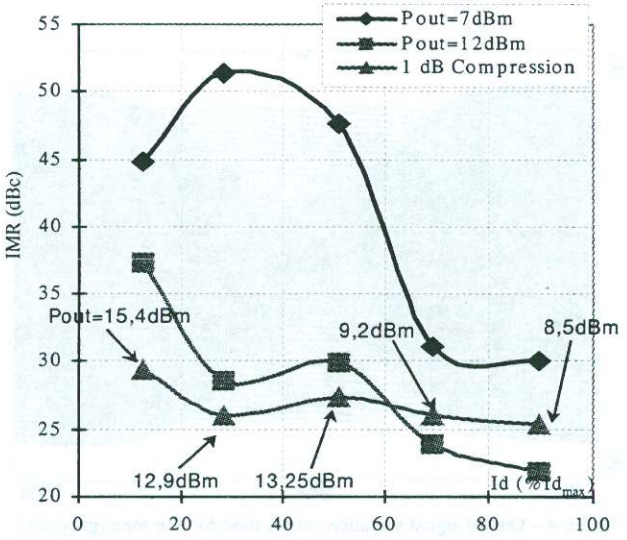

Figure 6 – IMR versus Id for Pout=7dBm, Pout=12dBm, and Pout=1dB power compression (Vds=5V)

contour and the corresponding IMR at 0.5dB below the maximum output power and at constant input power level

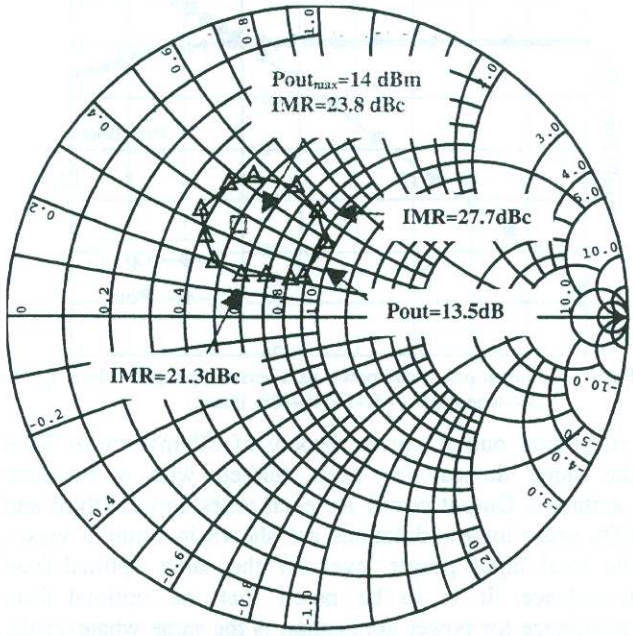

figure 7 – Constant output power contour and the corresponding IMR for a constant input power and Pout=Poutmax-0.5dB=8.2dBm

is shown (figure 7). It can be noted that the IMR could be improved of 4dB for an output power loss of only 0.5dB. The study of IMR as a function of the gate current for the same points as in figure 7 has shown a strong correlation between the two quantities. Some simulations will evaluate this dependence.

V. CONCLUSION

Measurements achieved using an accurate 26–40GHz on wafer intermodulation system were reported. These measurements are interesting from different aspects, first to optimize the device technology for linearity (reverse engineering), then to determine the optimal output load both for power and linearity. Modelling and simulations will help us to analyze these points

VI. REFERENCES

[1] C. Gaquière, E. Bourcier, B. Bonte, and Y. Crosnier " A Novel 26-40 GHz Active Load Pull System ", *25th European microwave conference procedings*, Vol 1, pp339-342

[2] C. Blair, " LDMOS Devices Provide High Power for Digital PCS ", *Applied Microwave and Wireless*, pp 84-88, october 1998

[3] R. S. Pengelly, *Microwave Field Effect Transistor. Theory and application*, pp 75-77

[4] R. Hajji, F Beauregard, F. Ghannouchi, "Multitone Power and Intermodulation Load-Pull Characterization of Microwave Transistors Suitable for Linear SSPA's Design" *IEEE Trans Microwave Theory Tech*, vol.45, pp 1093-1099, July 1997.