TECHNOLOGY AND THERMAL STABILITY OF ALGAN/GAN HFETs

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ABSTRACT

New approaches towards high reliable thermal stable ohmic and Schottky contacts for GaN/AlGaN-HFETs have been developed and implemented in device structures. The contact technology has been systematically optimized towards i) good electrical properties, ii) superior contact morphology and contour definition and iii) high reliability and thermal stability. HFETs employing source/drain contacts based on WSiN diffusion barriers sandwiched between an Ti/Al/Ti/Au internal layer system and an overlayer metal as well as WSiN/Au and Ir/Au gate contacts have demonstrated long term stability at 400°C. Even after temperature storage tests at 500°C no significant device degradation could be detected. Ir/Au Schottky gates have found to be stable at the rather high level of Schottky barrier height of about 1.1 eV resulting in dramatically reduced leakage currents as compared to standard Pt/Ti/Au gate contacts to GaN-HFETs.

INTRODUCTION

The characteristics of recently fabricated GaN-based FETs show the potential of III-nitrides for high power, high temperature and high frequency electronic applications. Significant progress in III-nitride epitaxy and device processing opened the way to high quality GaN based electronic devices like Junction Field-Effect Transistors (JFETs) [1], High Electron Mobility Transistors (HEMTs) [2, 3] and unintentionally doped Polarization Induced HEMTs (PIHEMTs) [4]. Even first remarkable results on Heterojunction Bipolar Transistors (HBTs) have been published recently [5]. The operation of AlGaN/GaN HFETs at elevated temperatures has been successfully demonstrated [6, 7]. According to an often expressed understanding high temperature electronics based on GaN-technology has the chance to promote to a significant market if the devices once demonstrate high performance, high reliability and high reproducibility [8].

However thermally stable ohmic and Schottky contacts to AlGaN/GaN HFETs pose an issue that is not sufficiently solved up to now. Additionally microwave and integrated circuit applications require a continuous scaling down of device dimensions. This in turn asks for metallizations with exact contact edge definition and high lateral homogeneity. Therefore investigations have been conducted towards thermally stable AlGaN/GaN HFETs employing new ohmic and Schottky contact systems that meet all these requirements.

Commonly used Ti/Al/Ti/Au ohmic contacts suffer from both thermal degradation and rough contact morphology [9]. A recent review on GaN contact technology is given by Liu [10]. Design strategies towards high temperature stable contact systems that have been demonstrated in GaAs-technology can be transferred to GaN to a certain extend. In particular WSiN diffusion barrier layers have been successfully used in GaAs high temperature electronics [11, 12] and can also be applied

as diffusion barrier layers for example between internal Ti/Al/Ti/Au ohmic contact layers to GaN and an Au overlayer or for Schottky contacts to GaN or AlGaN layers.

The thermal stability of Schottky gates in GaN/AlGaN HFET structures together with a reduction of gate leakage especially at elevated temperatures is of decisive importance. Transistors containing Pt based gates have shown strong degradation at elevated temperatures [9]. Therefore the development of an alternative gate contact metallization system being stable on high Al mole fraction AlGaN Schottky layers is of great interest. Here again the properties of WSiN are very promising to replace Pt based gate contacts. Sputtered Ir/Au contacts showed an even better performance with respect to the barrier height of the Schottky gate.

DEVICE PROCESSING

The AlGaN/GaN HFET structures used for our studies were grown by MOVPE on sapphire. On top of a GaN nucleation layer a 2.7 µm thick unintentionally doped GaN buffer layer and a 50 nm doped GaN channel was grown followed by a 3 nm $Al_xGa_{1-x}N$ spacer, a 15 nm $Al_xGa_{1-x}N$ doped supply layer, a 10 nm $Al_xGa_{1-x}N$ barrier layer (samples A and B: x = 0.2, samples C and D: x = 0.25, see Table 1) and a 1 nm GaN cap layer to prevent the top AlGaN from oxidation.

Device fabrication started with ohmic metallization, followed by device isolation, gate metallization and device passivation combined with pad metallization. Different sets of transistors containing conventional (A) and high temperature metallizations (B, C, D) (see Table 1) have been fabricated.

sample	Al content in AlGaN layers	Schottky contact metallization	Ohmic contact metallization
A	20 %	Pt/Ti/Au	Ti/Al/Ti/Au
B	20 %	WSiN/Au	Ti/Al/Ti/Au/WSiN
C	25 %	WSiN/Au	Ti/Al/Ti/Au/WSiN
D	25 %	Ir/Au	Ti/Al/Ti/Au/WSiN

Table 1: Al content in the AlGaN layers and Schottky contact metallization of the samples used for aging experiments

The conventional ohmic metallization contains a 20 nm Ti / 100 nm Al / 45 nm Ti / 55 nm Au metallization sequence. The ohmic contacts of the samples B - D consist of a 10 nm Ti / 50 nm Al / 25 nm Ti / 30 nm Au metallization followed by a reactively sputtered WSiN diffusion barrier layer (120 nm) to separate the internal metal system from the overlayer metal. The overlay metal is defined later in the process by the gate contact material. Due to the properties of the WSiN sputter deposition process the inner metals are totally embedded by WSiN (see Figure 1). Rapid thermal annealing (RTA) at 850 °C for 60 s was applied to activate the ohmic contacts. In contrast to ohmic source and drain contacts without WSiN the surface and the contours of the barrier containing contacts are smooth and well defined after annealing (Figure 2).

The gate fabrication was performed by optical lithography leading to a gate length of 1 µm. The gates are centered between source and drain (source-drain separaion: 4µm). For the Schottky contact of samples A 20 nm Pt / 50 nm Ti / 250 nm Au, for samples B and C 50 nm WSiN / 250 nm Au was employed. The gate metallization of sample D was based on a 50 nm Ir / 250 nm Au contact (Table 1). Device isolation was performed by combining reactive ion etching ($Ar/Cl_2/BCl_3$) and He

ion implantation. This resulted in comparably low surface leakage currents. Finally the samples were passivated with SiN_x. All aging experiments have been carried out at 400 °C in N_2 atmosphere.

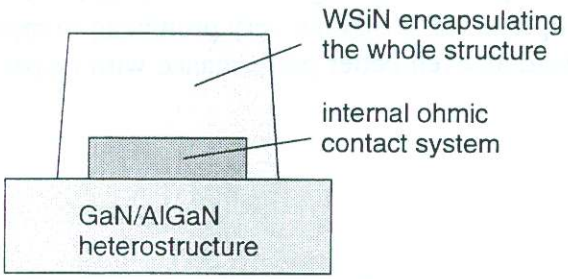

Figure 1: Schematic cross section of a high temperature ohmic contact to GaN completely embedded in a WSiN overlayer

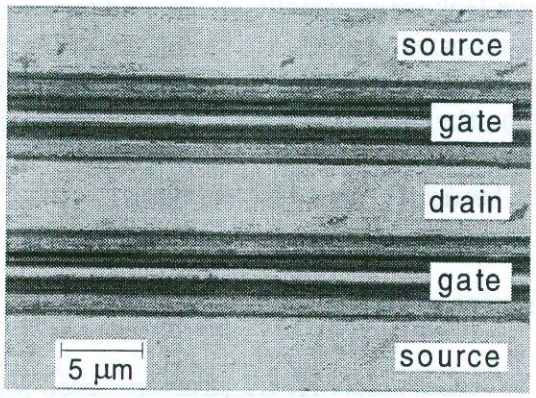

Figure 2: Microscope image of an AlGaN/GaN HFET after RTA at 850°C demonstrating the smooth contact surface and the good edge definition

RESULTS

The microscope image according to Figure 2 shows typical WSiN based ohmic source and drain contacts of samples B - D. Due to the properties of the WSiN sputter deposition process [9] the inner metal layers are entirely encapsulated by WSiN which suppresses the roughening of the underlying contact metallization during rapid thermal annealing. An important fact is that the WSiN barrier layer has to be thicker than the underlying contact metallization. Otherwise the WSiN barrier may crack during RTA and thus lead to interdiffusion effects accompanied by a drastic decrease of device yield and an increased ohmic contact resistance. The as prepared average values for the ohmic contact resistance R_c for sample A are 0.75 Ωmm and for samples B - D 0.62 Ωmm. After 24 h annealing at 400°C R_c increased to 0.95 and 0.77 Ωmm, respectively. The modified ohmic contacts show unchanged morphology with very well defined contact contours.

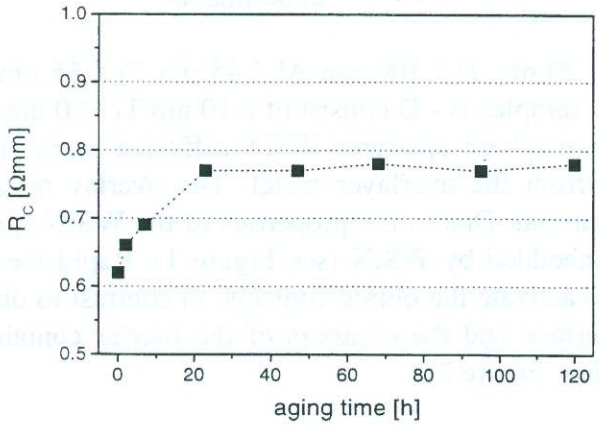

Figure 2: Ohmic contact resistance of WSiN based ohmic contacts versus aging time at 400°C (Ti 10nm / Al 50nm / Ti 25nm / Au 30nm / WSiN 120nm)

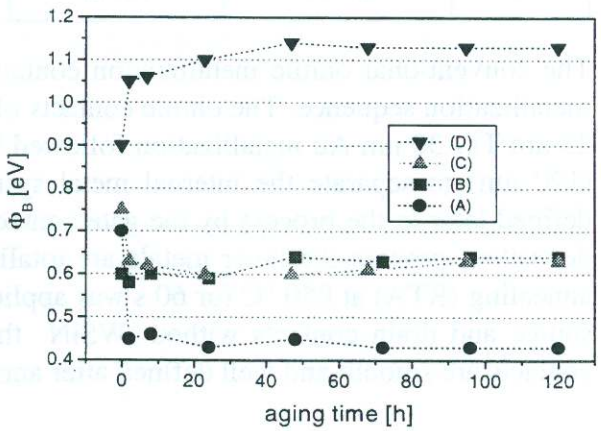

Figure 3: Schottky barrier height of different gate metallizations fabricated according to table 1 versus aging time at 400°C

The initial values of barrier height, maximum transconductance and maximum drain source current of the test transistors are given in Figures 3 to 5 respectively. The variations of the starting values are believed to be due to the different deposition modes of the individual gate metallizations.

During aging at 400°C the Pt-based gates of samples (A) strongly degrade resulting in a dramatical reduction of the Schottky barrier height to 0.45 eV within the first hours of annealing (Figure 3). This is associated with a decrease of g_m by 30% (Figure 4). After further long term annealing the barrier height stabilizes at this very low level while g_m and I_{DSS} decrease continuously although no increase of the transistor source resistance is observed (Figures 4, 5).

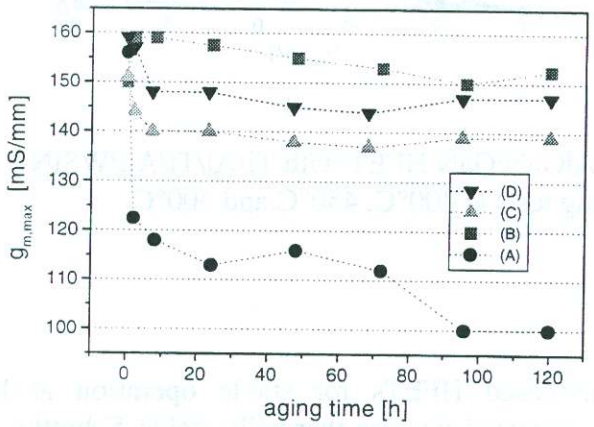

Figure 4: Maximum extrinsic transconductance versus aging time (Parameter: Contact structures according to table 1)

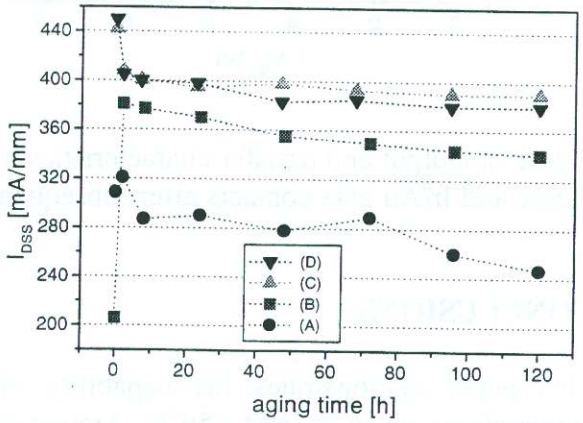

Figure 5: Maximum drain-source current versus aging (Parameter: Contact structures according to table 1)

HFETs employing WSiN/Au gates (sample B and C) show only a slight decrease of I_{DSS} and $g_{m,max}$ (see Figures 3, 4) even after 120 hours annealing at 400°C. For both structures the Schottky barrier height remained stable at around 0.65 V. The highest Schottky barrier height was measured for the Ir/Au Schottky metallization on $Al_{0.25}Ga_{0.75}N$ epitaxial layers (sample D). After the first aging steps the barrier height increases from 0.9 to 1.1 eV and stabilizes at this level even for long term annealing (120 hours) at 400°C (Figure 3). The leakage currents of these samples are almost two orders of magnitude lower than of transistors with WSiN/Au gate metallization (type C). From X-ray diffraction no change of the Ir/Au microstructure was observed. I_{DSS} and g_m of samples D initially decreased only by 7% and remained unchanged up to the end of the aging experiment (Figure 3, 4). Even after aging the output characteristics showed a very good pinch off behaviour (I_{DS} < 10 nA/mm).

Subsequent aging tests at 400°C, 450°C and 500°C were performed to evaluate the principal stability of the devices. Figure 6 shows the results of these investigations. The observed parameter variations are within less than 5% of the initial values if annealed up to 450°C. The first annealing at 400°C results in a slight shift of the maximum transconductance towards lower gate-source voltage. Further annealing at 450 °C nearly reproduced the initial values, whereas annealing at 500°C seems to cause slight degradation effects. Nevertheless in all cases the variations with respect to the initial values are less than 10% indicating very stable thermal properties.

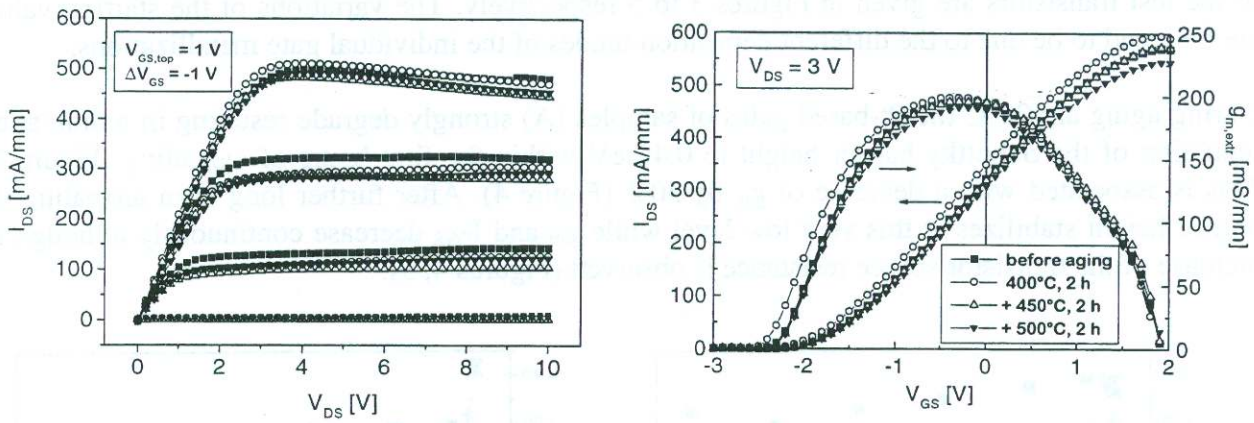

Figure 6: Output and transfer characteristics of an AlGaN/GaN HFET with Ti/Al/Ti/Au/WSiN ohmic and Ir/Au gate contacts after subsequent aging tests at 400°C, 450°C and 500°C.

CONCLUSIONS

This paper demonstrates the capability of GaN-based HFETs for stable operation at high temperatures up to at least 450°C. Among others, prerequisites are thermally stable Schottky and ohmic contacts with good surface morphology. Therefore new, improved contact systems have been developed using WSiN as a diffusion barrier for ohmic contacts and WSiN and Ir respectively for the Schottky contacts. In the case of ohmic contacts the WSiN layer completely encapsulates the internal Ti/Al/Ti/Au ohmic layer leading to thermally stable contacts with good surface morphology. WSiN and Ir based metallizations for gate contacts to GaN/AlGaN HFETs proved superior stability and electrical performance and are therefore a powerful alternative to conventional Pt based Schottky contacts that give rise to a strong degradation during long term aging at 400°C. The highest value of the Schottky barrier height Φ_B (1.1 eV) in combination with the lowest gate leakage currents could be achieved by the metal combination Ir/Au. These results open the way towards high reliable GaN-HFETs. Indeed, long term storage tests at 400°C demonstrated stable properties for more than 120 hours short term high temperature tests at 450°C and 500°C did not indicate catastrophic failures.

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