Multigigabit Programmable Comb Decimator implemented in GaAs/AlGaAs HEMT Technology

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Abstract — The architecture and design of a GaAs multi-GHz two-stage programmable decimator are presented. A transistor-level realisation of the first stage(the comb decimator) and the cell count of the second stage decimator in a 0.3 μm GaAs/AlGaAs HEMT E/D process are considered. The performance has been calculated through measurements made on two 12-bit adders using SDCFL and DCFL gates. An alternating carry state technique allows a speed of 2GHz to be obtained with 2.2W power dissipation from the comb decimator; the transistor count is 4525.

I. INTRODUCTION

Advances in VLSI technology have pushed forward the speed and resolution of state-of-the-art Analog-to-Digital Converters (ADCs), with high resolution and high speed commonly being achieved using oversampling (sigma-delta) techniques. For high resolution at video frequencies (above 10MHz) these techniques demand gigahertz sampling rates, and consequently multi-GHz decimator circuits are required to produce the output. This paper describes the implementation of a 2GHz two-stage decimator circuit to meet this requirement, with a decimation ratio programmable from 8 to 64.

II. DECIMATOR ARCHITECTURE

One of the most attractive architectures for integrated very high frequency decimating circuits uses a multi-rate system having a first-stage comb decimator stage followed by a half-band FIR filter [1]. The comb decimator consists of R stages of comb filters and a sampling rate compressor, where R is chosen to give the required attenuation in the stopband. The transfer function of this R-stage filter in the Z-domain is: $H(z)=\left[\frac{1-z^{-N}}{1-z^{-1}}\right]^{R}$ where N is the order of the comb filter and is equal to the first stage decimation factor (M_1). All the coefficients in a comb filter are equal to unity, so neither multipliers nor coefficient storage are needed, resulting in a VLSI efficient realisation. The following FIR filter should compensate for the roll-off error in the baseband and provide a sharp cut-off to prevent aliasing in the following signal compressor. The comb filter can be realised by R accumulators in series, which provide a $1/(1-z^{-1})^{R}$ function, followed by a compressor (using compression ratio N) and R differentiators, which together give a $(1-z^{-N})^{R}$ function [1]. The central accumulator and differentiator can be combined with the compressor and replaced by a simple accumulate-and-dump circuit [2].

The accumulators in this structure require a long word size to prevent overflow. This can be remedied by using modulo arithmetic and setting the length of the accumulator and differentiator registers equal to the output word length so as to create a structure that is insensitive to overflow [3]. Using the two's complement number system, the required number of bits is given by: $B = 1 + R * \log_2 M_1$. For a second-order ΣΔ modulator, a three-stage comb filter is needed [3]. Decimation by 16 therefore requires a three-stage comb filter having 13-bit adders and latches. The accumulators must all operate at the gigahertz rate of the input bit-stream, although in the differentiators the data rate is much lower, and slower components can be used. The first accumulator can be realised as a fast counter enabled by the input stream; the subsequent accumulators require two high speed 13-bit adders. The complete comb decimator circuit is shown in Fig. 1; a programmable frequency divider allows the oversampling ratio to be adjusted from 8 to 64 in steps of 8.

III. LOGIC

Operation at multi-gigahertz rates requires ultra-high speed transistors, and GaAs IC technologies are favoured due to their inherent speed-power advantage over silicon technologies. For LSI applications, the GaAs Source-Coupled Logic (SCFL) family generally provides highest speed, but can consume excessive power. Table I shows the total number of components (N) and the maximum propagation delay (t_{dmax}) of a simulated 13-bit all-EFET SCFL adder using HSPICE and parameters for the Fraunhofer 0.3 μm GaAs/AlGaAs HEMT E/D process [4]. High speed is achieved, however the power dissipation is also very high. SCFL gates also need two anti-phase signals for the inputs and outputs which increases the layout area.

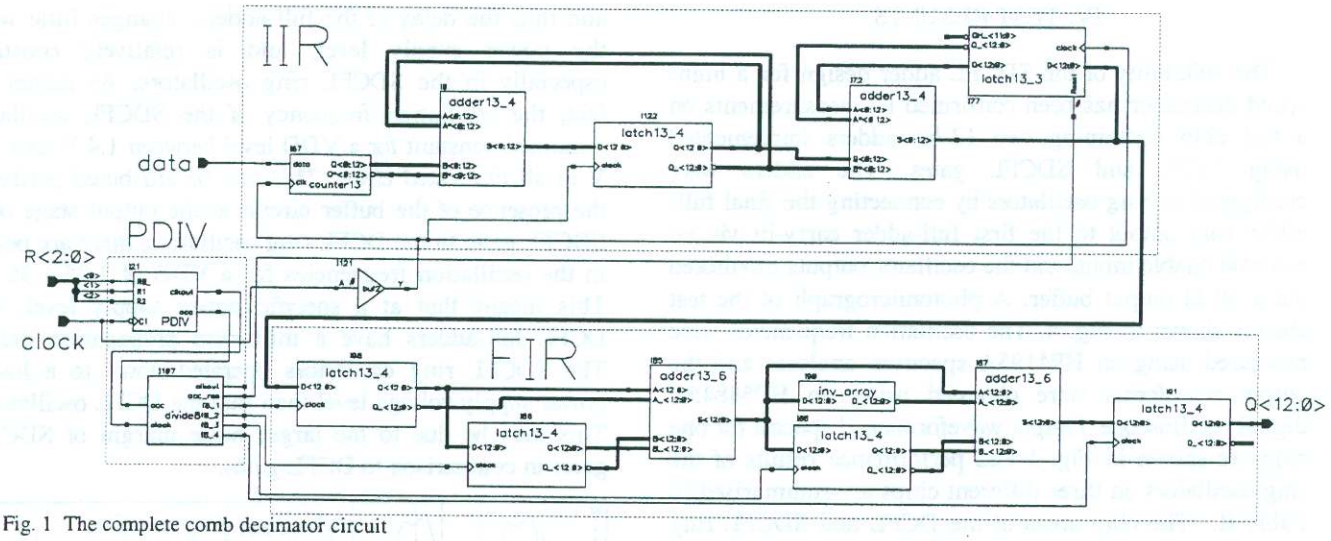

Fig. 1 The complete comb decimator circuit

Reduced area and power dissipation can be obtained using the GaAs Direct-Coupled FET Logic (DCFL) family, although DCFL suffers from a small noise-margin so that circuits are restricted to using NOR gates only. This can lead to large gate counts and propagation delays, as shown by the simulation results for a 13-bit DCFL adder in Table I, although the power dissipation is reduced. A DCFL adder is not suitable for a multi-GHz comb decimator even if carry look ahead (CLA) logic is added to increase its speed.

The speed can be improved using 'source-follower DCFL (SDCFL)' or 'buffered E/D' logic (Fig. 2). SDCFL offers an improved noise margin, reduced delay, and is much less sensitive to process parameter variations than DCFL. More significantly it allows the implementation of complex gate functions such as AOI, OAI, and XOR without major increases in the number of devices or the power dissipation, and gate outputs can also be wire-ORed together.

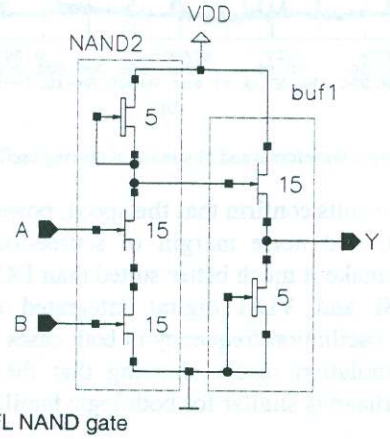

Fig. 2 SDCFL NAND gate

The availability of complex gates means that a full-adder need use only 7 SDCFL gates (Fig. 3) in comparison to 15 DCFL gates. This SDCFL full-adder requires an active high carry-in and generates an active low carry-out, so it would seem that extra inverters are needed if full-adders are to be cascaded. However, inverting the inputs to the carry generator circuit and converting an AOI gate to a OAI gate will make the carry-out state active high. By alternating the carry-out state in adjacent stages of the 13-bit adder circuit a reduced propagation time can be achieved. The simulation results in Table I show that the number of transistors and thus the area are low, along with the power dissipation and the maximum propagation delay.

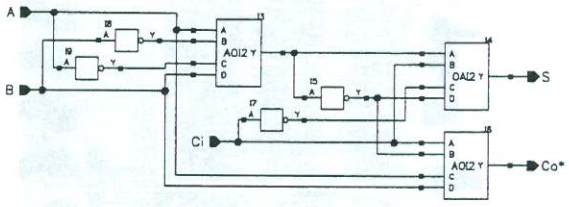

Fig. 3 A SDCFL full-adder

A faster 13-bit SDCFL adder can be built using three 4-stage carry-look-ahead (CLA) adder circuits and the sum part of a SDCFL full-adder circuit. The alternating-carry technique can again reduce the carry propagation time. The simulated performance is given in Table I. This ultra high speed adder can achieve the same speed as the SCFL adder but with a much lower power dissipation. Although the numbers of components are similar, the total SDCFL chip area will also be less than the SCFL realisation since the SCFL adder needs two tracks for each input or output.

TABLE I
The performance of the 13-b adders

	N	P_{disp}(mw)	t_{dmax}(ps)
SCFL cascade adder	600	409	185
DCFL cascade adder	598	258	558
SDCFL cascade adder	481	196	389
SDCFL CLA adder	603	211	187

IV. TEST RESULTS

The suitability of the SDCFL adder design for a high-speed decimator has been confirmed by measurements on a test chip containing two 12-bit adders implemented using DCFL and SDCFL gates. The adders were configured as ring oscillators by connecting the final full-adder sum output to the first full-adder carry-in via an external enable input, and the oscillator outputs monitored via a 50 Ω output buffer. A photomicrograph of the test chip is shown in Fig. 4. The oscillation frequencies were measured using an HP4195A spectrum analyser and the output waveforms were obtained using an HP54845A digital oscilloscope. Output waveforms and spectra for one chip are shown in Fig. 5 and performance results of the ring oscillators on three different chips are summarised in Table II. The chip areas of the DCFL and SDCFL ring oscillators are 0.52 and 0.36 mm^2, respectively. A figure of merit, η, can be defined to compare the performance of the adders, where $\eta = \frac{frequency}{area \cdot power}$. The η values are also given in Table II. The simulation results gives $\frac{\eta_{SDCFL}}{\eta_{DCFL}} = \frac{3.3}{1}$ and the average value of $\frac{\eta_{SDCFL}}{\eta_{DCFL}}$ on the tested chips is $\frac{2.7}{1}$.

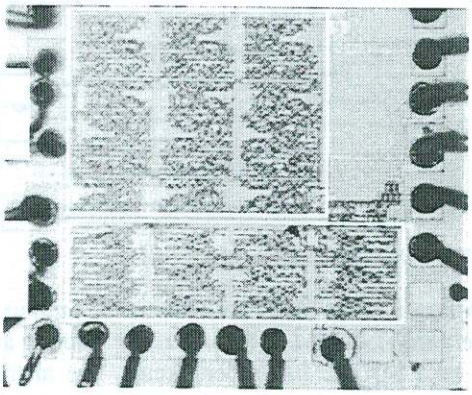

Fig. 4 Photomicrograph of the test chip

The output frequency versus the power supply voltage level in both oscillators are illustrated in Fig. 6 for the tested chips. The measurements can be used as an indication of propagation delay variation with the power supply level and to determine the minimum power supply voltages in which the ring oscillators are functioning properly. The measurements were carried out for the power supply level up to 1.8 V. The oscillation frequency and thus the delay of the full-adders changes little with the power supply level, and is relatively constant especially in the SDCFL ring oscillators. As matter of fact, the oscillation frequency of the SDCFL oscillator remained constant for a VDD level between 1.4 V and 1.8 V in all the tested chips. This can be attributed partly to the presence of the buffer circuit at the output stage of a SDCFL gate. In the DCFL ring oscillators, there are peaks in the oscillation frequencies for a VDD of 1.25-1.35 V. This means that at a specific power supply level, the DCFL full-adders have a minimum propagation delay. The SDCFL ring oscillators operated down to a lower power supply voltage level than that the DCFL oscillators. This may be due to the larger noise margin of SDCFL gates in comparison to DCFL gates.

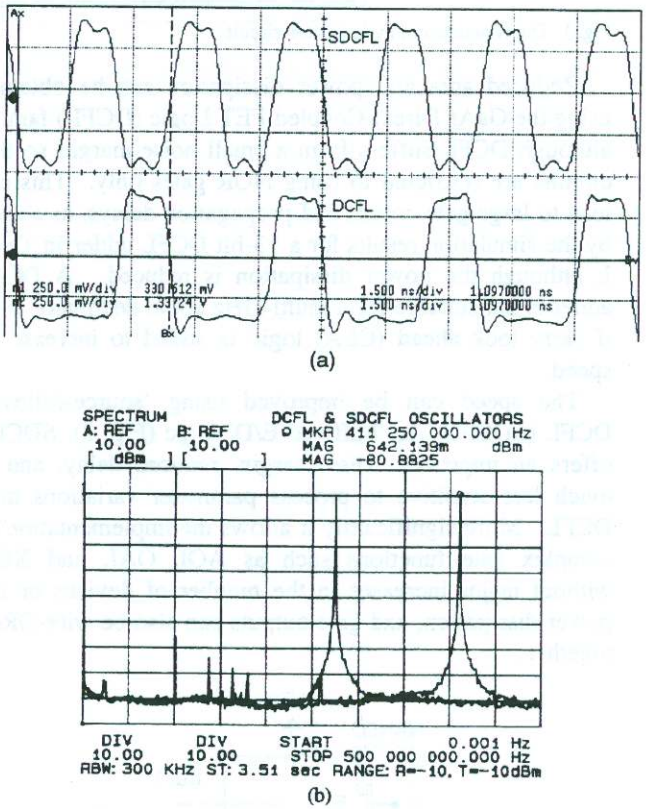

Fig. 5 a) Output waveforms and b) spectra of the ring oscillators in chip B

These results confirm that the speed, power dissipation, chip area, and noise margin of source-follower DCFL (SDCFL) make it much better suited than DCFL for use in GaAs LSI and VLSI digital integrated circuits. The measured oscillation frequency in both cases is about 46% of the simulation result, showing that the interconnect delay overhead is similar for both logic families.

TABLE II

The measured and simulated performance of the ring oscillators

	Chip A		Chip B		Chip C		simulation	
	DCFL	SDCFL	DCFL	SDCFL	DCFL	SDCFL	DCFL	SDCFL
P_{disip}, mW	228	183	234	183	235	185	276	179
f_{osc}, MHz	267	394	275	412	266	390	610	897
η, MHz/mW · mm^2	2.25	5.98	2.26	6.25	2.17	5.86	4.25	13.92
η_{SDCFL}/η_{DCFL}	2.7		2.8		2.7		3.3	

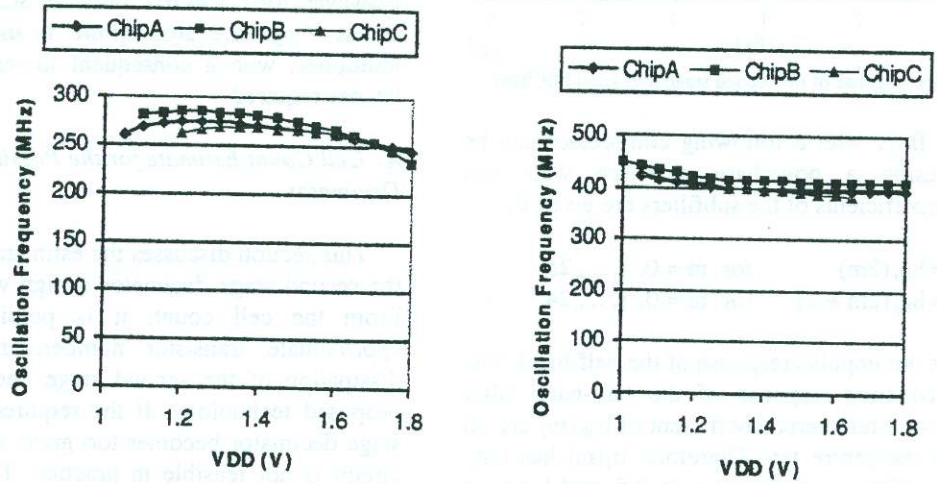

Fig. 6 Output frequencies versus the power supply level for a) the DCFL and b) the SDCFL ring oscillator

V. COMB DECIMATOR

A comb decimator based on the fast SDCFL adder has been designed using the Fraunhofer 0.3 µm GaAs/AlGaAs HEMT E/D process [4]. The layout shown in Fig. 7 occupies an area of 8 mm^2 and requires 4525 transistors. The data flows from left to right in the filter and the carries propagate from top to bottom through the adders. Using air bridges with the second level metal significantly reduces the parasitic capacitance of the interconnections [4]. HSPICE Simulation predicts a maximum delay path of 248 ps; the measured high speed adder test circuits suggest that this will be increased to approximately 500 ps by interconnect delays. The comb decimator can thus be expected to operate with sampling frequencies up of 2 GHz. The total power dissipation will be 2.2 W.

VI. A POSSIBLE GAAS HALF-BAND FIR FILTER DESIGN FOR THE SECOND STAGE DECIMATOR

The perfect solution to the design of the second stage decimator is to use a half-band FIR filter in which almost half of the impulse response coefficients are zero, and the coefficients are symmetrical around the centre-tap whose value is 0.5. The frequency response of a half-band filter which meets the desired specification is illustrated in Fig. 8. The filter length is 51 and the coefficient size is 11 bits.

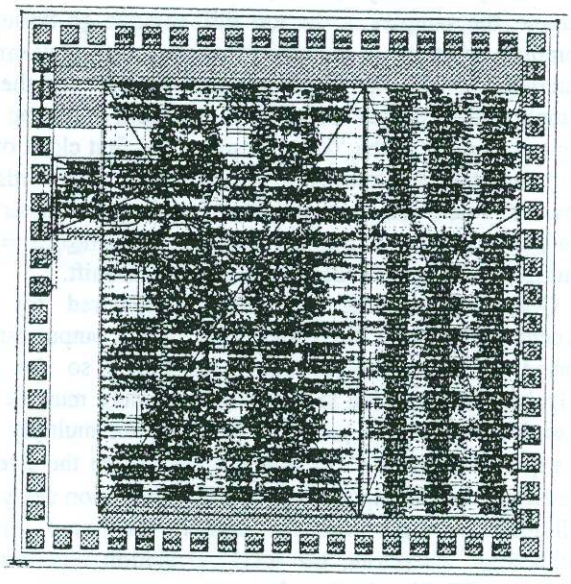

Fig. 7 The complete comb decimator layout

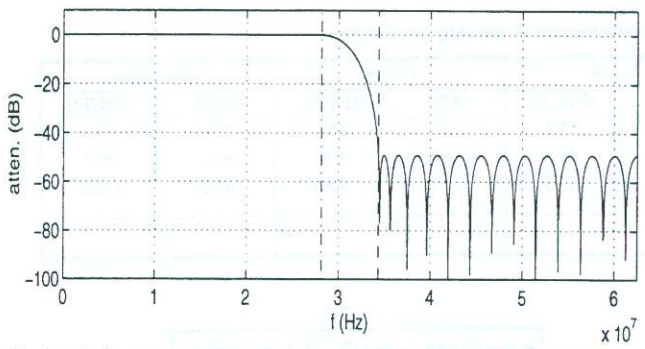

Fig. 8 The frequency response of the second stage half-band FIR filter

A half-band filter with a following compressor can be implemented using a polyphase structure with two subfilters. The coefficients of the subfilters are given by

$$h_0(m) = h_{hb}(2m) \quad \text{for } m = 0, 1, ..., 25$$
$$h_1(m) = h_{hb}(2m + 1) \quad \text{for } m = 0, 1, ..., 24$$

where $h_{hb}(m)$ is the impulse response of the half-band. The symmetrical frequency response of the half-band filter implies that the odd-numbered coefficient of $h_{hb}(m)$ are all zero expect for the centre tap. Therefore, $h_1(m)$ has only one non-zero coefficient whose value is 0.5, and $h_0(m)$ is symmetrical, so the implementation of the filter is extremely simple. Since the compressor is embedded into the polyphase structure, the computation is performed at the Nyquist rate (f_s/M).

A symmetrical FIR structure, depicted in Fig. 9, can be used to realise the second-stage decimator. The even-numbered impulse response coefficients are stored in a Read-Only Memory (ROM) and for each new input sample, the samples in the top shift register go through a complete rotation. At the start of phase 0, one new sample enters the lower path of the top shift register and the last sample in this register enters the higher path of the top shift register. S stays at the '0' state only at the first clock of the shift register and returns to the '1' state afterwards. In phase 1, a new sample enters the bottom shift register and there is no rotation in this shift register. Since $h_{hb}(25) = 0.5$, multiplication by this coefficient is a simple shift.

Only one parallel multiplier is required for this structure. For f_s = 2GHz and M = 32, the output sample period of the whole decimator is 16 ns so the total calculation time in the second stage structure must be less than this period. In a parallel multiplier, the multiply time is approximately $(X+Y)\tau$ where X and Y are the sizes of the two multiplier inputs and τ is the propagation delay of a full-adder in the chosen digital integrated circuit technology. Therefore, the total calculation time for the half-band FIR filter is given by :

$$T_{hb} \approx \frac{N(X+Y)\tau}{4}$$

Where N is the filter length (= 51) and only N/4 products are calculated for each input. For X = S + 1 = 11 (the width of summation of two input samples) and Y = C = 11 (the filter coefficient size), τ must be less than 57 ps. According to the data given in Table I, the required one-bit full-adder propagation delay can easily be met by all the logic families (SCFL, DCFL, and SDCFL) in the IAF HEMT process. The choice of logic family can be made on other design factors such as power dissipation and area. However, for f_s = 4GHz, only the SCFL family can be used unless a systolic architecture is used to implement the multiplier, with a consequent increase in the number of latches required.

A. Cell Count Estimate for the Possible Second Stage Decimator

This section discusses the estimation of the cell count of the second stage decimator design with a half-band filter. From the cell count, it is possible to calculate the approximate transistor number, die area, and power dissipation of the second stage decimator design in the proposed technology. If the required area for the second stage decimator becomes too great, then fabrication of the circuit is not feasible in practice. The cells used for this design are from the SDCFL or DCFL logic family dependent on the application. This choice keeps down the power dissipation of the whole design. As discussed earlier, both logic families can be used for f_s = 2GHz. The cell count is initially calculated based on MSI cells such as D-type latches and full-adders, and subsequently the approximate transistor number, power dissipation, and area are derived.

The second stage decimator structure, illustrated in Fig. 9, is mainly composed of two shift registers, an arithmetic unit (including a parallel multiplier and an accumulator), and the coefficient ROM. The shift registers are S bits wide and total 3N/4 words in length so 3NS/4 DCFL D-type latches are required to implement them. The parallel multiplier can be realised approximately by XY = C(S + 1) DCFL full-adders [5]. The multiplier output is (S + C + 1) bits wide and N/4 products are added together in the accumulator for each input, so the accumulator and output adders require $ceil(\log_2 \frac{N}{4}) \cdot (S + C + 1)$ full-adders (ceil(x) rounds the elements of x to the next highest integer). The accumulator register requires the same number of latches. The adder after the top shift register needs (S + 1) full-adders.

The coefficient ROM can be implemented with multiplexers. A N/4:1 multiplexer is required for each coefficient bit. The address bit width is $ceil(\log_2 \frac{N}{4}) = 4$. The required number of DCFL NOR gates for each 13:1

multiplexer, is approximately twice the number in a full-adder. The total approximate cell count, transistor number, and power dissipation for the second stage decimator are given in Table III .

The total estimated number of transistors is 21000 and the required die area is approximately 32 mm^2. Moreover, excessive heat will be generated by the power dissipation of 10.5W. A CMOS or BiCMOS digital integrated circuit technology must be used to realise the second stage.

VII. CONCLUSION

This paper described the complete design, simulation, and implementation of a programmable multi-GHz two-stage GaAs HEMT decimator using source-follower DCFL (SDCFL) complex gates. Test chips containing high-speed DCFL and SDCFL adders have been fabricated by Fraunhofer IAF and tested. The measurement results suggest that 2GHz operation of the comb decimator can be achieved. For a total decimation factor of 32, the comb/FIR decimator output will provide 56 dB dynamic range at 64 MHz. This performance is suitable for the realisation of a complete oversampling ADC IC offering high resolution at video frequency output rates.

The implementation of the second-stage FIR filter on the same chip is not feasible at present because of other limiting factors such as power dissipation and die area. Therefore, a single-chip solution for the whole multi-GHz decimator cannot be achieved.

VIII. ACKNOWLEDGEMENTS

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IX. REFERENCES

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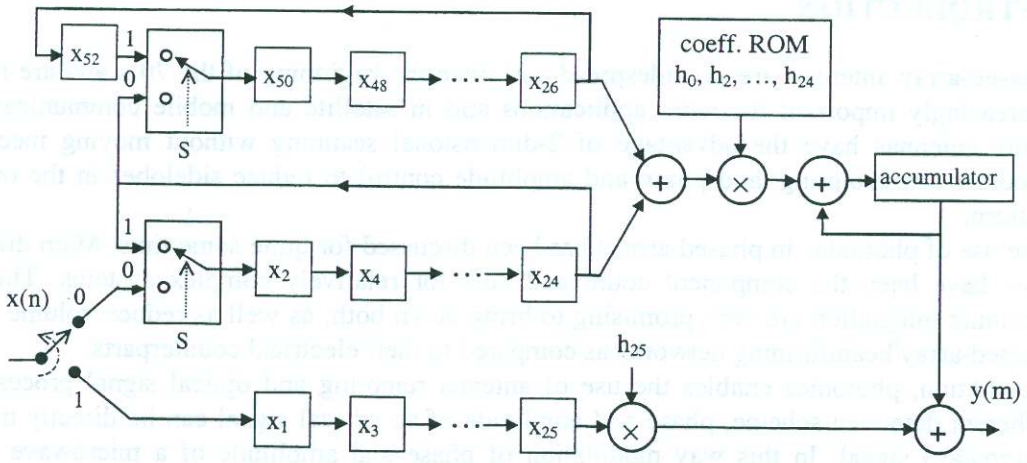

Fig. 9 The second stage decimator structure

TABLE III
The cell count for the possible second stage decimator

Sections	Cells	Transistors	P_{dissp} (W)
Shift registers	3NS/4 D-latches	7410	3.510
Parallel multiplier	C(S + 1) full-adders	3751	1.936
Adders	8(S+C+1) + (S+1) full-adders	5797	2.992
Accumulator latch	4(S+C+1) D-latches	1672	0.792
ROM	2C full-adders	682	0.352
Control circuitry	plus 10% of the total cells	1688	0.918
Total	-	21000	10.5