

A COMPACT BROADBAND HIGH EFFICIENT X-BAND 9-WATT PHEMT MMIC HIGH-POWER AMPLIFIER FOR PHASED ARRAY RADAR APPLICATIONS

A.P. de Hek, P.A.H. Hunneman, M. Demmler* and A. Hülsmann*

TNO Physics and Electronics Laboratory, P.O. Box 96864, 2509 JG The Hague, The Netherlands
Phone: 31.70.374.04.09, Fax: 31.70.374.06.54, Email: deHek@fel.tno.nl

* Fraunhofer Institute for Applied Solid State Physics, Tullastr. 72, 79108 Freiburg, Germany

Abstract-In this paper the development and measurement results of a compact broadband 9-Watt high-efficient X-band high-power amplifier are discussed. The described amplifier has the following state-of-the-art performance: an average output power of 9 Watt, a gain of 20 dB and an average Power Added Efficiency of 35% over a relative bandwidth of 40% at X-band. The amplifier is realised in a pseudomorphic HEMT GaAs MMIC technology developed by the Fraunhofer Institute for Applied Solid State Physics (FhG-IAF) in the scope of the WEAG/TA1/CTP8.1 program.

INTRODUCTION

Component costs are of vital importance for the successful development of Transmit Receive (TR) modules for phased array radar applications. One of the key components of a Transmit Receive module is the high-power amplifier. The performance of such an amplifier must be optimised not only in electrical performance but also with respect to cost. For this reason we decided to integrate the driver and high-power amplifier normally found in TR modules onto one single chip. To make this feasible a technology has to be used that has per transistor a high output power combined with a high gain. Such a technology is the pseudomorphic HEMT (PHEMT) technology developed by FhG-IAF in the scope of the WEAG/TA1/CTP8.1 program. This program aims at the development of X-band high-power amplifiers in MESFET and PHEMT technologies. The work within this program is carried out by a consortium consisting of Siemens (now Infineon), Thomson Detexis, FhG-IAF, IEMN and TNO-FEL. Earlier work obtained in the scope of the before mentioned program is reported in [1,2].

The development of a high-power amplifier starts with the selection of the technology and the unit size of the transistors. After the transistor is selected, it must be modelled and the optimum load impedance must be de-

termined. This will be discussed in more detail in the next section. After the transistor modelling the high-power amplifier design and measurement results are discussed.

TECHNOLOGY

The pseudomorphic HEMT process of FhG-IAF is used for the development of the discussed amplifier [3]. This process is optimised for high-power applications. The process consists of: 0.3 μm PHEMTs, E-beam gate technology, MIM capacitors and airbridges. The viaholes and backside processing of the presented amplifier are performed by Infineon.

To reduce the occupied chip area as much as possible PHEMTs with a fishbone layout have been used, see figure 1. The main advantage of this layout is the fact that the total gate width of the transistor can be increased, and thus the output power of the HPA, without significantly increasing the occupied chip area.

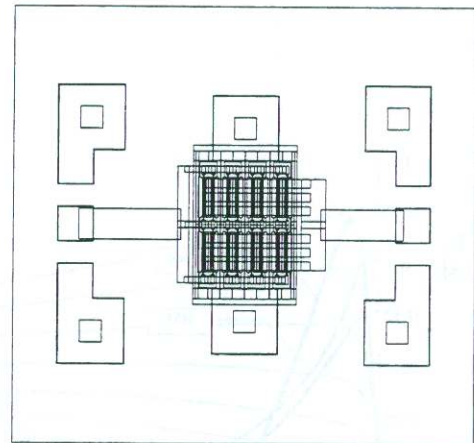


Figure 1: Fishbone FET layout used in the discussed HPA (total gate width is 1.44 mm).

As large-signal transistor model the EEHEMT1 model of HP-EEsof is used. The model parameters are determined with the help of XTRACT from HP-EEsof. After the transistor model is established, the bias voltages and the location of the optimum load impedance are determined with the help of the active load-pull measurement system described in [4,5]. A comparison between the large-signal measurement and simulation results is shown in figure 2.

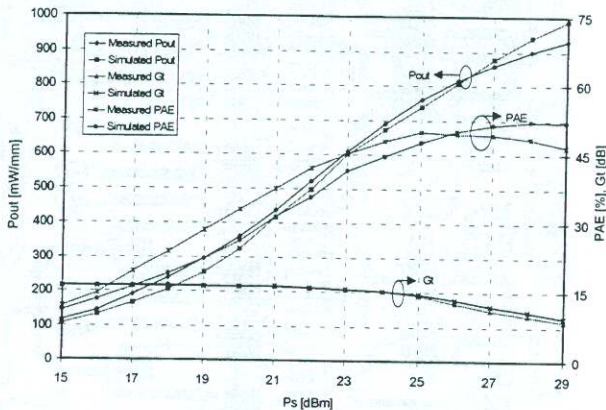


Figure 2: Comparison between large-signal measurement and simulation results of a 1.4 mm PHEMT ($f=8$ GHz, $V_d=8$ V, $V_g=-0.4$ V).

The results show that a saturated output power of more than 900 mW/mm is measured. Furthermore a power added efficiency (PAE) maximum of 50% and a gain of more than 16 dB are measured. This indicates that it is possible to design a compact high-power amplifier that has both a high output power and a high PAE.

The results depicted in figure 2 also show that there is a good agreement between the predicted and the measured large-signal performance of the transistor.

AMPLIFIER DESIGN

A two-stage HPA is designed. This HPA uses eight fishbone FETs in parallel in the output stage. These FETs have a total gate width of 11.52 mm. In the input stage four fishbone FETs are used that have a total gate width of 5.76 mm.

For the design of the matching networks it is important to have accurate models available of the microstrip discontinuities. It was already shown in [6] that the T-junction model available in Libra is not accurate enough for power amplifier design on GaAs wafers with a thickness of 100 μ m. Besides the T-junction model also the 45° microstrip bend [4], the 90° microstrip bend and the microstrip

crossing turn out to be not accurate enough. To circumvent this problem, scaleable microstrip models are determined with the help of electromagnetic field simulations. For these simulations MOMENTUM from HP-EEsof is used. Besides the before mentioned microstrip discontinuities also a model is determined for a scaleable Y-junction. This discontinuity is not available in Libra but is very useful for the realisation of compact matching networks. In figure 3 the root mean square error between the measured and simulated results of a 100 μ m wide symmetrical Y-junction is shown.

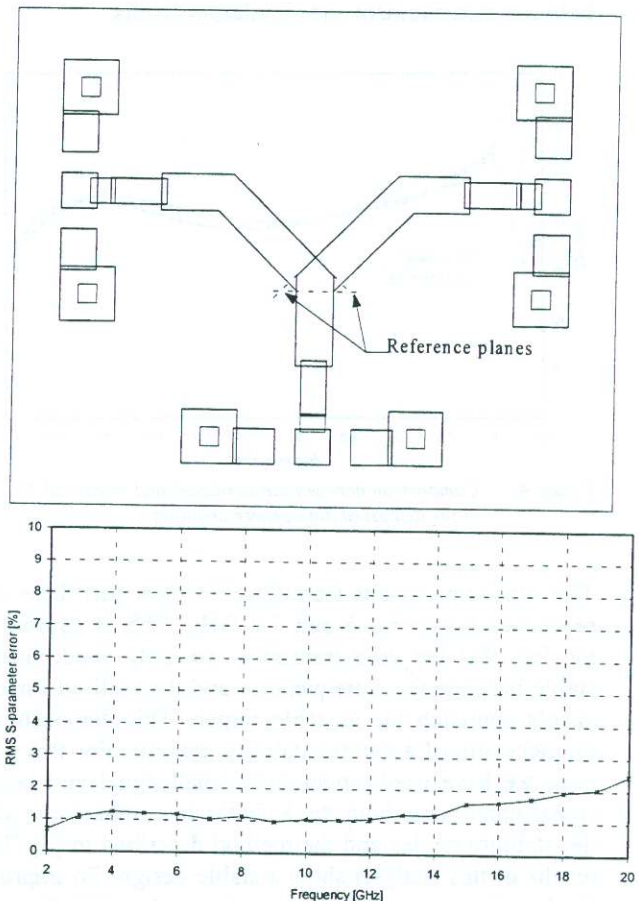


Figure 3: Layout test structure and Root Mean Square S-parameter error of a symmetrical Y-junction with a line width of 100 μ m.

The measured and simulated S-parameters are compared at the reference planes shown in figure 3. The results show that there is an excellent agreement between the measurement and simulation results. This is also an excellent demonstration of the capabilities of electromagnetic simulations for microstrip based HPA design. Besides the discontinuities also the coupling between the various parts of the amplifier must be taken into account. This is clear if we have a look at the amplifier layout depicted in figure 5.

The design information necessary for the matching networks is for the output matching network obtained from load-pull measurements. The necessary information for the design of the input and interstage matching networks are obtained from large-signal simulations with the help of the transistor model. The before mentioned amplifier design method, where both electromagnetic field simulations and a large-signal transistor model are used, leads to excellent results. Prove of this can be seen in figure 4. In this figure the simulated S21 is compared to the measured S21. The results show that there is an excellent agreement between measurement and simulation results.

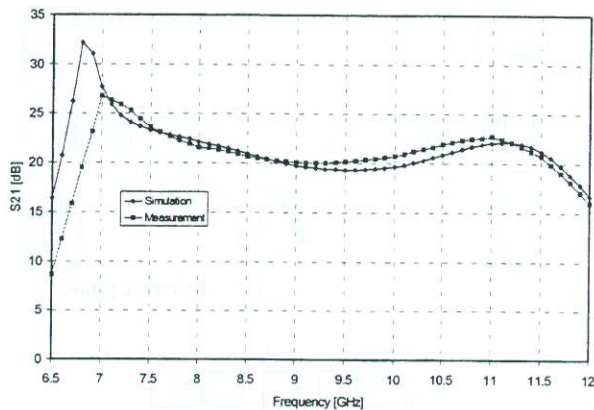


Figure 4: Comparison between the simulated and measured S21 of the discussed high-power amplifier.

The simulation results from figure 4 show that there is a resonance between 6.5 and 7.0 GHz. This is caused by the fact that the used transistors are only conditionally stable between these frequencies and the realised impedance's approach the unstable region. This demonstrates the necessity of a careful stability analysis. For this purpose we have used, under both small-signal and large-signal conditions, both the k-factor in combination with the stability circles and the method described in [7]. The results of this analysis show a stable design. To improve the low frequency stability margin on-chip 500Ω resistors have been placed to ground at all transistor gates and drains.

MEASUREMENT RESULTS

A photograph of the realised high-power amplifier is depicted in figure 5. The realised amplifier has a size of only 16 mm^2 . This small size makes it clear that it is possible to realise a combined driver and high-power amplifier with the help of the PHEMT technology of FhG-IAF.

Some typical measurement results, obtained at different locations on the wafer, are depicted in figure 6. The results show, for a drain-source voltage of 8 V, that from 7.0 to 11.0 GHz an average output power of 6.5 Watt, an average PAE of 34% and a gain of more than 21 dB has been measured.

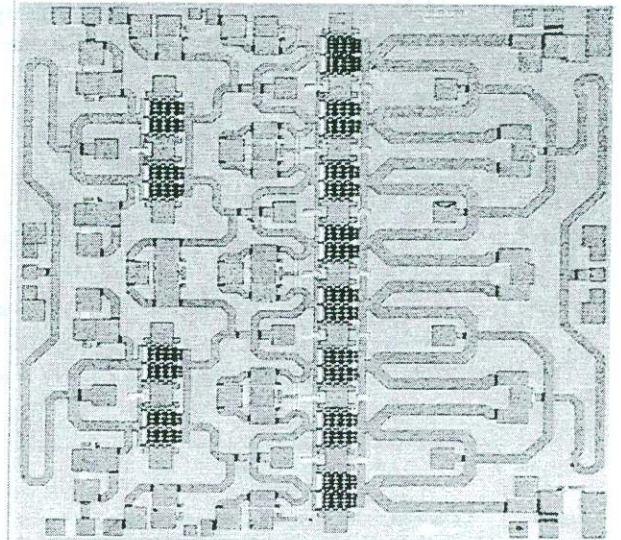


Figure 5: Photograph of layout high-power amplifier ($4 \times 4 \text{ mm}^2$).

The results from figure 6 also show that the maximum variation in the measured output power is approximately 0.5 dB over the frequency band of interest.

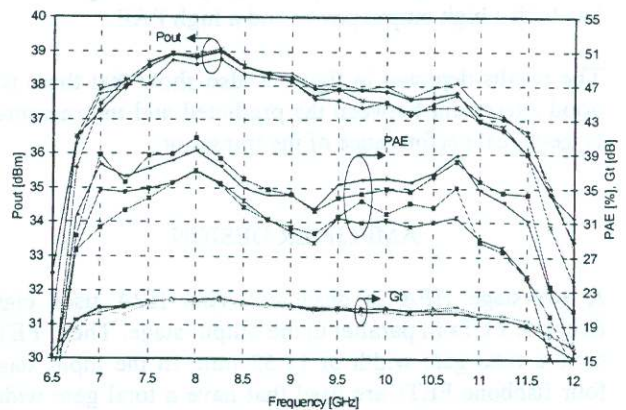


Figure 6: At different locations on the wafer measured large-signal performance high-power amplifier. ($V_{ds}=8 \text{ V}$, $V_{gs}=-0.3 \text{ V}$, Pulse width= $10 \mu\text{s}$ and PRF= 20 kHz).

Before mentioned results are obtained under pulsed conditions. However the discussed high-power amplifier must also be able to function also under CW conditions. In figure 7 the pulsed and CW measurement results are compared at a drain voltage of 8 V. The results show that

the measured output power in the CW mode is not more than 1 dB less than in the pulsed mode. This is quite good especially when we note that no special precautions have been taken to cool the amplifier in the CW mode. The absence of cooling resulted in an increase of the ambient temperature of the amplifier from 25 °C to 55 °C. From the depicted results can be concluded that an average output power of 5.2 Watt, an PAE of 32% and a gain of more than 20 dB has been measured in the CW mode over the 7.0 - 11.0 GHz frequency band.

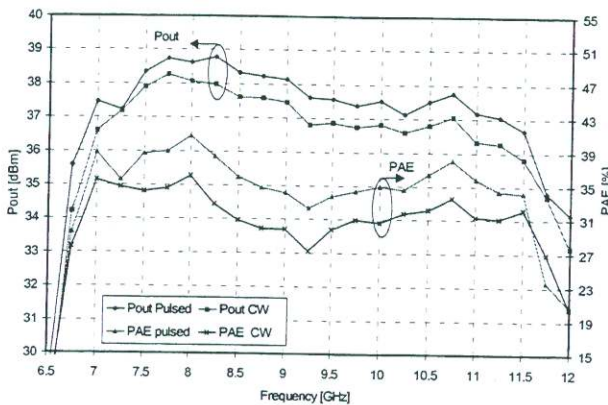


Figure 7: Comparison CW and pulsed high-power amplifier measurement results. ($V_{ds}=8\text{ V}$, $V_{gs}=-0.3\text{ V}$, Pulse width=10 μs and PRF=20 kHz).

The application, for which the amplifier is designed, requires a drain voltage of 8 V. However due to the high break-down voltage (>20 V) of the used process, it is also possible to use the amplifier at higher drain voltages.

The measurement results of a typical sample measured at three different drain voltages are depicted in figure 8. The results show that from 7.5 to 11.5 GHz an average output power of 9 Watt and an average PAE of 35% has been obtained. The gain of this HPA is 20 dB over the frequency band mentioned before.

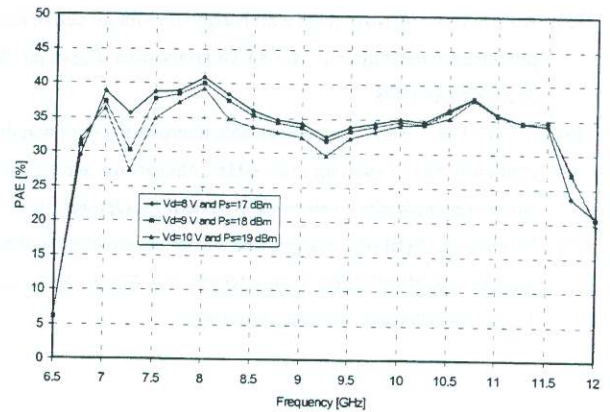
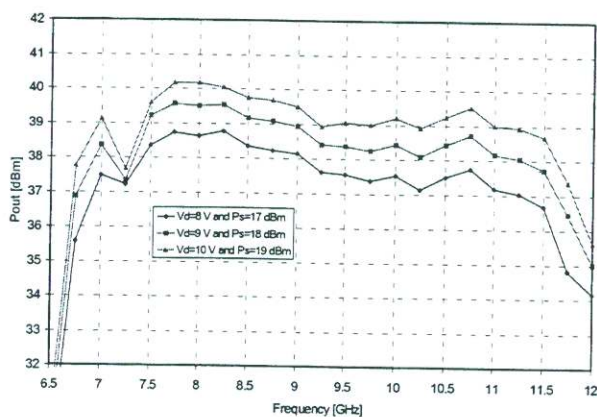


Figure 8: Comparison pulsed high-power amplifier measurement result at three different drain voltages. ($V_{gs}=-0.3\text{ V}$, Pulse width=10 μs and PRF=20 kHz).

CONCLUSIONS

With the help of a European PHEMT technology a state-of-the-art compact high-power amplifier has been developed that is suited for application in future TR modules for phased array radar applications. The feasibility to realise a single chip driver and high-power amplifier with the help of PHEMT technology has been demonstrated.

The measured results show an average output power of 9 Watt, a PAE of 35% and a gain of 20 dB over a relative bandwidth of 40% at X-band.

REFERENCES

- [1] F.L.M. van den Bogaart, A.P. de Hek and A. de Boer, "MESFET High-power High-Efficiency Amplifiers at X-band with 30% bandwidth", *GAAS96 proceedings*, pp. 3A2-1 - 3A2-4, June 1996
- [2] A.P. de Hek, F.L.M. van den Bogaart, "Broadband High Efficient X-band MMIC Power Amplifiers for Future Radar Systems", *Wocsdice 97, 21st Workshop on Compound Semiconductor Devices and Integrated Circuits proceedings*, pp. 63 - 64, May 1997
- [3] W. Marsetz, A. Hülsmann, K. Köhler, M. Demmler and M. Schlechtweg, "GaAs PHEMT with 1.6 W/mm output power density", *Electronics Letters*, pp. 748 - 749, April 1999
- [4] F.L.M. van den Bogaart, A.P. de Hek, "First-pass Design Strategy for High-Power Amplifiers at X-band", *IEE Tutorial Colloquium on "Design of RFICs and MMICs digest"*, pp. 8/1 - 8/6, November 1997

- [5] A.P. de Hek, "A Novel Fast search algorithm for an active load-pull measurement system", *GAAS'98 symposium digest*, pp. 268 - 273, October 1998
- [6] A.P. de Hek, "An Accurate Scaleable microstrip T-junction discontinuity model valid up to 50 GHz", *Microwave and Communication Technologies Conference proceedings*, October 1997
- [7] M. Ohtomo, "Stability analysis and numerical simulation of multidevice amplifiers", *IEEE Trans. Microwave Theory Tech.*, vol. 41, pp. 983-991, no. 6/7, June/July 1993