# 94-GHz Low Noise Amplifier on InP in Coplanar Technology

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*Abstract* - **High performances have been achieved at W-band with a 2-stage 0.1 µm gate-length InGaAs/InAlAs/InP LM-HEMT MMIC low noise amplifier in coplanar technology. To obtain the T-gate profile, we use silicon nitride $Si_xN_y$ technology, which leads to naturally passivated devices. For a drain-to-source current Ids=350mA/mm the devices demonstrate a maximum intrinsic transconductance Gm of 1600mS/mm and an intrinsic current gain cutoff frequency Fc=220GHz. The extrinsic current gain cut-off frequency Ft is 175GHz. The LNA shows a minimum noise figure of 3.3dB with an associated gain of 11.5dB at 94GHz.**

## I. INTRODUCTION

The increase of applications such as LMDS, LANs, satellite constellations as well as passive imaging systems demands the realization of high performance low noise amplifiers. InP-based HEMTs have demonstrated very high cutoff frequencies and low noise figures making then very suitable InAlAs/InGaAs transistors for applications in the W-band. In this paper, we present the fabrication and the performance of W-band monolithic 2-stage low noise amplifier based on lattice-matched HEMT devices. The gate process is especially developed for millimeter wave integrated circuits at W-band frequencies using coplanar wave-guide technology.

## II. DEVICE PROCESSING

The MMIC amplifier was fabricated on a lattice-matched InAlAs/InGaAs HEMT active layer grown by molecular beam epitaxy in our laboratory using a solid source MBE 2300 Riber system. This structure consists of an InAlAs buffer layer, an undoped InGaAs channel, an InAlAs spacer, a single Si planar doping layer, an InAlAs schottky layer and finally a heavily doped InGaAs cap layer. At room temperature, the square resistance is 190Ω/□, the sheet carrier density is 3.48 $10^{12}cm^{-2}$ and the electron mobility is $9600cm^2/v/s$. At 77K, the square resistance is 60Ω/□, the sheet carrier density is 3.45 $10^{12}cm^{-2}$ and the electron mobility is $32000cm^2/v/s$.

The processing steps were optimized to provide high performance devices and a high yield. The devices were isolated using mesa etching with a $H_3PO_4$:$H_2O_2$:$H_2O$ solution. To prevent gate-leakage current problems, we selectively etch the InGaAs channel at mesa sidewalls with SA(succinic acid):$H_2O_2$ solution. Ohmic contacts were then realized by evaporating Ni/Ge/Au/Ni/Au metal followed by a 295°C, 20s, rapid thermal annealing under $N_2/H_2$ atmosphere. The device was then covered up with 800Å silicon nitride film deposited by PECVD. This dielectric layer protects the active zone and supports the top of the T-shaped gate and is also used as the dielectric of MIM capacitors. The 0.1µm gate length footprint was defined by electron-beam lithography using PMMA and $Si_xN_y$ etching using a highly non-isotropic $CF_4/CHF_3$ RIE process. The top of the gate (0.3µm) was then defined using a (PMMA-P(MMA-MAA)) bilayer resist. Gate recess was performed in a SA:$H_2O_2$ wet etching solution followed by Ti/Pt/Au metal evaporation [1]. A SEM

cross section is shown in Fig.1. To avoid reverse-side processing, coplanar waveguide technology is chosen for the passive circuitry. Metallic resistors consist of a 700Å of Ti leading to a sheet resistance of 16Ω/□. To define the CPW ground to ground spacing (d=70μm), a trade-off between losses and low dispersion up to W-band was considered. The line attenuation is about 0.4dB/mm at 94GHz for a 50Ω transmission line. Electro-plated air-bridges were added at each discontinuity in order to suppress the undesired slot-line mode. The air-bridges were designed to introduce low parasitic effects over the whole W-band.

## III. DEVICE MODELING

The amplifier was designed by Thomson-Detexis using accurate broadband models from a complete library of CPW passive elements developed at I.E.M.N. and validated up to 110GHz [2]. This library includes matching networks (symmetric, asymmetric, bended stubs), metal resistors, MIM capacitors (serie, shunt), DC-blocks and step impedance lines. These models do not use measured S-parameter fittings, but are based on Heinrich's CPW line model [3], which needs geometrical data and physical process parameters only. Each slice of transmission line, resistance or capacitance is modelled by a R-L-C-G equivalent circuit. For metal resistors and MIM capacitors, experimental DC resistance and low frequency capacitance measurements are also needed. The complete distributed model was implemented into ®Hewlett Packard's Microwave Design System (MDS).

In order to design low noise circuits in the millimeter wave range, reliable broad-band small signal models of the active devices are required. The small signal equivalent circuit of 0.1μm LM-HEMT was determined from S-parameter measurements for a number of gate widths and DC drain current densities. A complete database was then developed allowing to optimize the gate width and DC drain current of the LM-HEMT used in the two-stage amplifier.

The new "two temperatures" noise model proposed by G. Dambrine [4] was used for the design of the low noise amplifier. In this model, the device noise performance is calculated using two uncorrelated noise sources, an input voltage noise source $e_{in}$, and output current noise source $i_{out}$. Two equivalent noise temperatures $T_{in}$ and $T_{out}$ are defined respectively from these two noise sources. One property of the model states that $T_{out}$ is directly related to the drain current while $T_{in}$ is constant and close to the ambient temperature. Moreover, these two temperatures are independent of the gate width, which is well suited for circuit design.

## IV. RESULTS

- The devices reported in this paper have been optimized for high gain operation at W-band. Fig.2 shows a typical dc *I-V* curve of the 0.1μm InP-HEMT which exhibits excellent pinch-off voltage of Vp=-0,4V. A peak extrinsic transconductance $Gm_{ext}$ greater than 1100 mS/mm at Vds=1V can be observed in Fig.3. The extrinsic current gain cutoff frequency Ft seen Fig.4 is 175GHz. The small-signal equivalent circuit was extracted from the measured S-parameters in the 1-50GHz frequency range. Fig.5 presents the small-signal equivalent circuit as a function of the drain-source current. We obtain a maximum transconductance Gm of 1600 mS/mm and an intrinsic current gain cutoff frequency Fc=220GHz for a drain-to-source current Ids=350 mA/mm. We can note that Gm and Fc remain high even at low values of drain current (1050 mS/mm and 175GHz respectively at 100 mA/mm).

- Fig.6 shows a photograph of the complete realized W-band two stage CPW amplifier. The chip size is 1.7mmx1.5mm. S-parameters noise figure and associated gain of amplifiers were characterized using on-wafer techniques. The measured data $S_{21}$ and $S_{22}$ of the two-stage LNA are presented in Fig.7. The gain, which demonstrates 11.5dB at 94GHz, is shown from 75 to 110GHz. The output return loss value, better than 12dB from 86 to 96GHz, is 14dB at 94GHz. The isolation is better than 24dB from 75 to 110GHz. The noise figure and associated gain performance measured at 94GHz are shown in Fig.8 for different amplifiers and biasing conditions. At 94GHz, the best LNA demonstrates a minimum noise figure of 3.3dB with an associated gain of 12.2dB which is excellent performance for a low noise amplifier

using coplanar wave guide technology operating in W band.

## V. CONCLUSION

We have developed a high performance two-stage InP HEMT MMIC low noise amplifier with 0.1µm gate length in coplanar technology. At 94GHz, the best LNA demonstrates a minimum noise figure of 3.3dB with an associated gain of 12.2dB.

## VI. ACKNOWLEDGEMENTS

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Fig.1. SEM image of a 0.1 µm gate deposited on the silicon nitride layer.

## VII. REFERENCES

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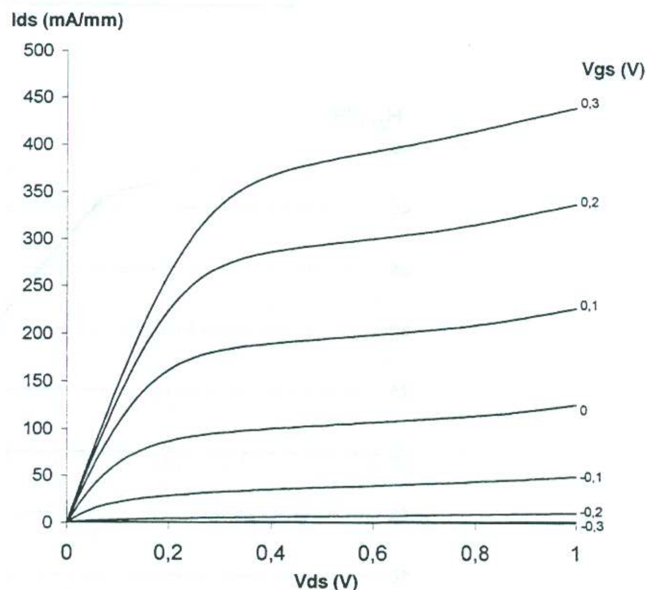


Fig.2. DC (I-V) curve of 0.1µm InGaAs/InAlAs LM-HEMT device demonstrating good pinchoff characteristics.

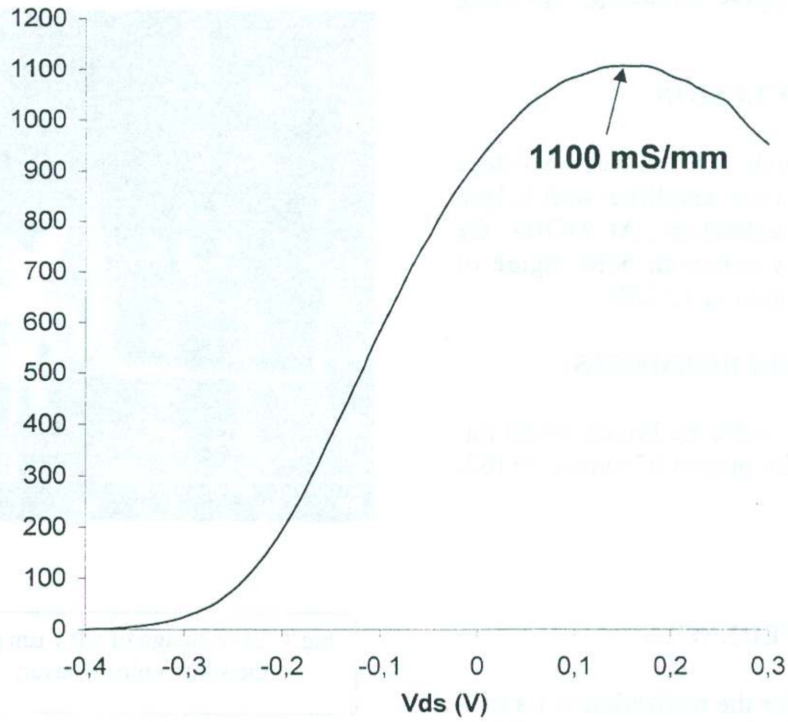


Fig.3. Extrinsic transconductance $Gm_{ext}$ for Vds=1V

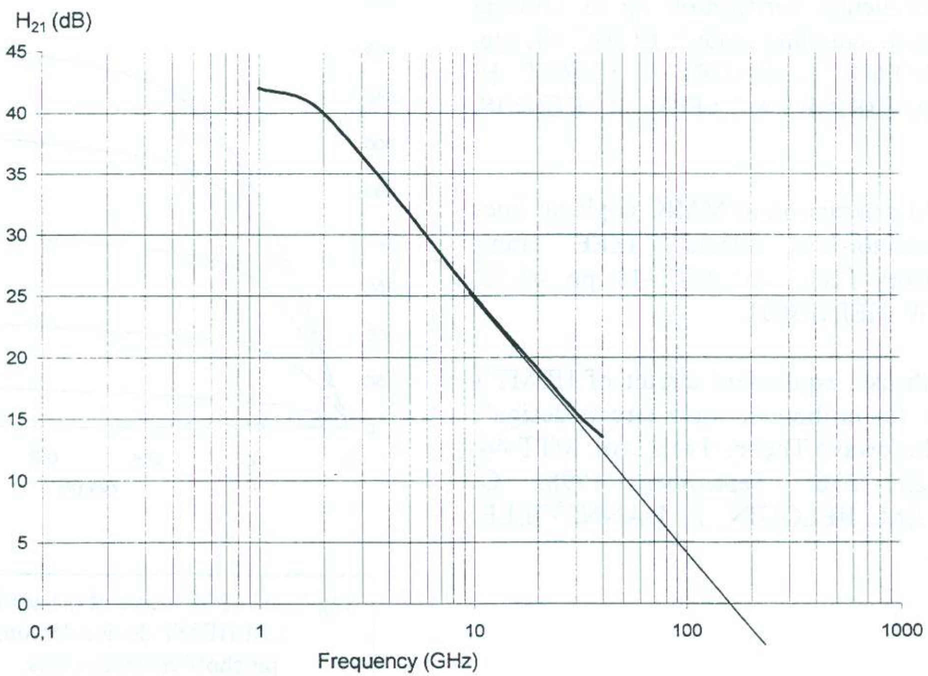


Fig.4. Extrinsic current gain cutoff frequency Ft

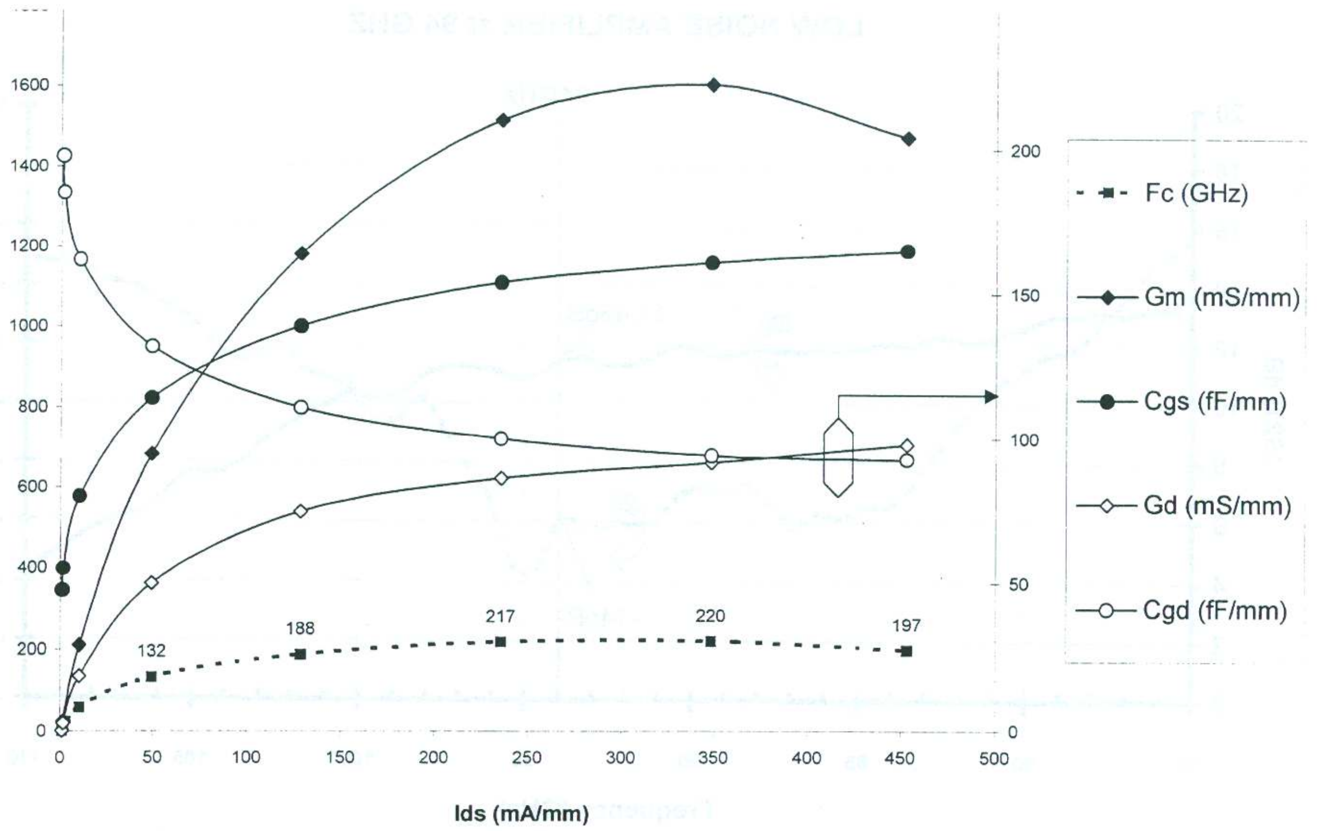


Fig.5. Elements of the small signal equivalent circuit (–◆–◊–•–o– ■ –)Gm, Gd, Cgs, Cgd, Fc

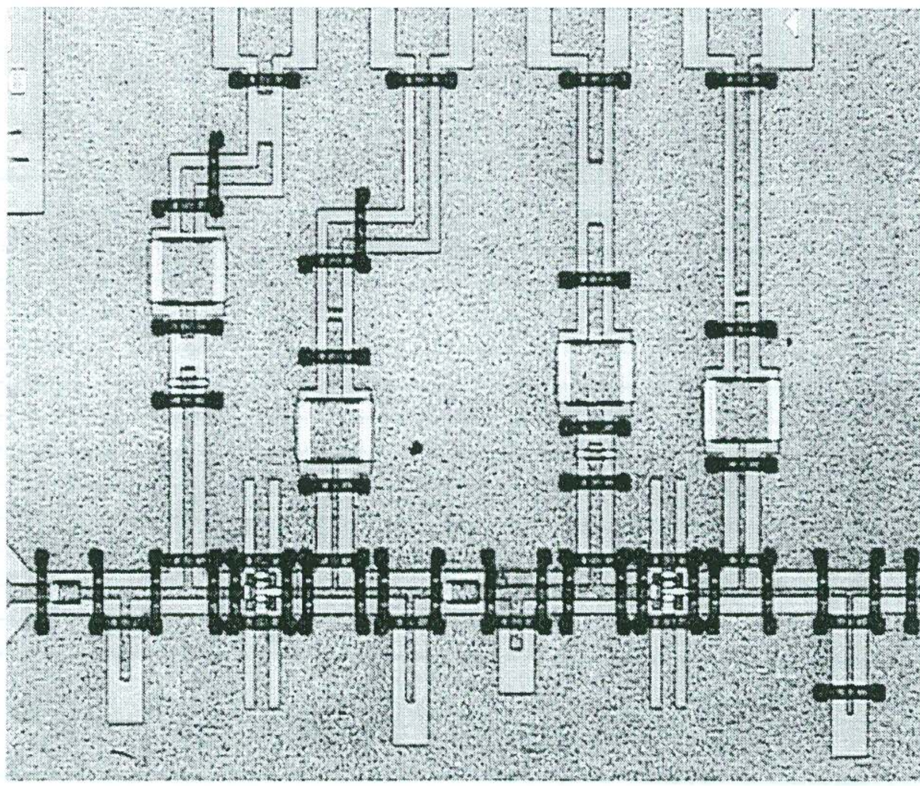

Fig.6.Topology of the realized two stage CPW amplifier

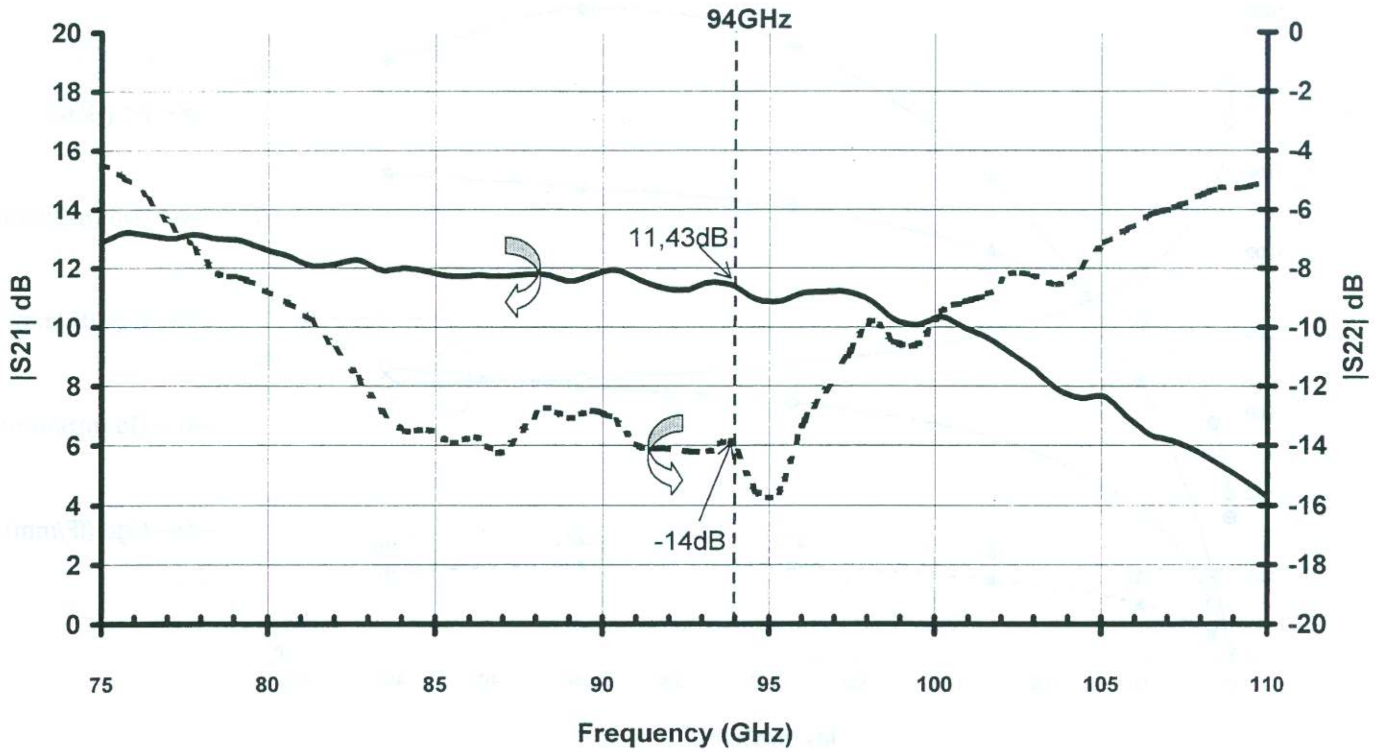


Fig.7 Measurements results of the W-band two-stage for optimised biases

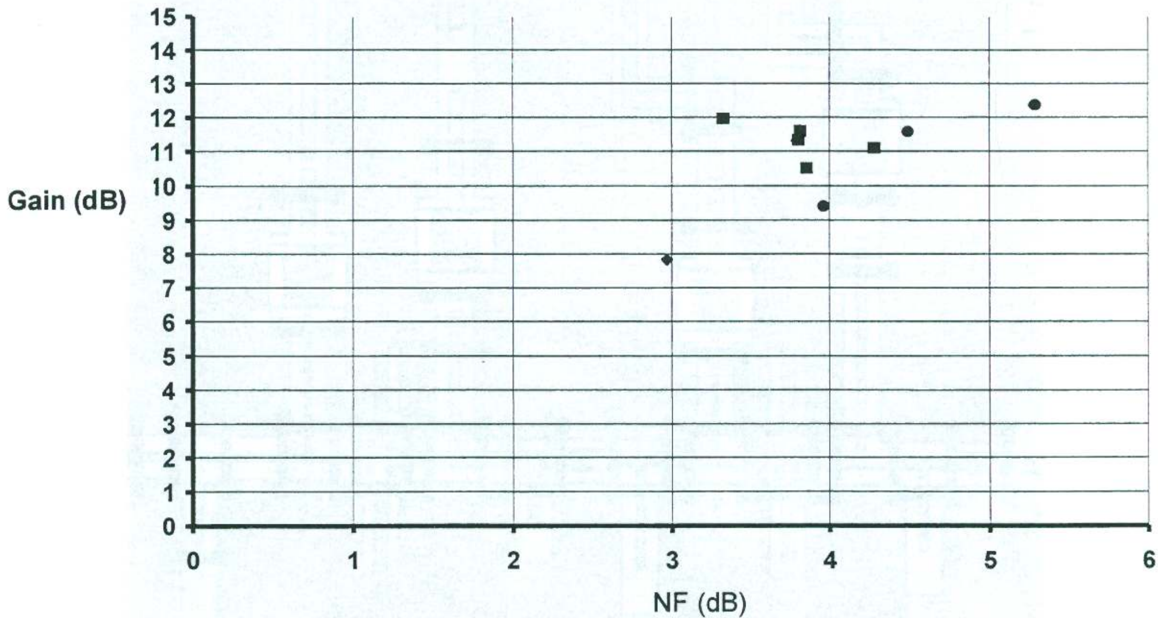


Fig.8. Noise figure and gain measured at 94 GHz for the two-stage CPW amplifier. Uncertainty is about 0.2 dB for both noise figure and gain