A TWO-DIMENSIONAL ELECTROTHERMAL MODEL FOR GaAs MESFETs

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Abstract – **A new physical-based electrothermal model for GaAs MESFET is presented. The 2-D electrical model based on the accurate velocity-electric field Chang-Fetterman expression is coupled to a thermal simulator which is able to take into account the thermal dependence of GaAs thermal conductivity and the multilayer structure of a typical chip. The simulator has been compared with the results of a 3-D FDM simulator and measurements. The accuracy is to be considered satisfactory and the CAD tool can easily perform the simulation on a common PC.**

I. INTRODUCTION

The accurate prediction of the peak and average temperature of GaAs MESFETs, especially in power circuits, has become one of the main priority in device and circuit design and analysis. Peak temperature has a great influence on the reliability and lifetime of the circuit, and the operative average temperature affects the forecast of the microwave and steady-state electrical behavior.

In this paper a two-dimensional thermal model is proposed and coupled to a two-dimensional physical-based electrical model so as to perform the electrothermal simulation by a common PC, achieving, at the same time, the highest accuracy as possible. The model takes into account the electrothermal feedback between current and temperature, the temperature-dependent GaAs thermal conductivity and all the layers under the semi-insulating GaAs substrate (die-attachment, mounting, heat sink) and over it (epoxy layer, coating) are considered together with the thermal convection with the still air.

Section II presents a brief state-of-the-art of thermal simulators, whereas in Section III the physical-based model is described. The results of the simulations are compared with a 3-D FDM simulator and measurements in Section IV. Section V summarizes the contents of this paper.

II. STATE-OF-THE-ART OF THERMAL SIMULATORS

The problem of the heat spread in power GaAs devices was widely studied by many researchers in the past [1-15]. They presented many physical-based models to perform the computation on the available systems, often powerful workstation, and, at the same time, obtain accurate, meaningful and reliable results.

The full resolution of the 3-D static heat flux equation:

$$\nabla \cdot \left[k_{TH}(T) \nabla T(x,y,z) \right] = -P(x,y,z,T,t) \qquad (1)$$

in which ρ is the density of the material, c is the specific heat, t is the time, k_{TH} is the temperature-dependent thermal conductivity, T the temperature and P the dissipated power density, is in most cases of interest, too CPU expensive. Thus, the Kirchhoff transformation was used to linearize the problem (1), shifting the non-linearity from the flux equation to its boundary conditions [1]. In spite of this simplification, the electrothermal 3-D problem with an arbitrary power source is often too heavy to be solved.

A great simplification was obtained by dividing the thermal source in a suitable set of elementary sources (hot spot, square or circular source) and applying the superposition principle of effects to find the final temperature field [2,3]. Thus, it was possible to avoid the complexity of the shape of the source and then to extract a simpler solution of the linearized 2-D or 3-D static problem:

$$\nabla^2 T = -P/k_{TH} . \qquad (2)$$

There are two basical approaches to solve Eq. (1) or (2): either a numerical or an analytical solution. In the former case there are some good examples of thermal simulators based on the finite-element (FEM) [4] or finite-difference (FDM) [5,6] or boundary-element method (BEM) [7]. Those are the most popular numerical approaches to solve a non-linear partial differential equation but many problems concerning the computational load could raise. The foregoing methods are, in fact, very sensitive to the resolution of the spatial grid in the crucial section of the device, i.e. the active layer, so it becomes very time-consuming to simulate with the required accuracy a whole three-dimensional multifinger structure taking into account the top and bottom layers (coating layer, metallizations, die-attachment, mounting, heat sink),

as shown in Fig. 1. This task is particularly hard to perform on a PC-based system, so that specialized mathematical tool-box and powerful workstations are to be used.

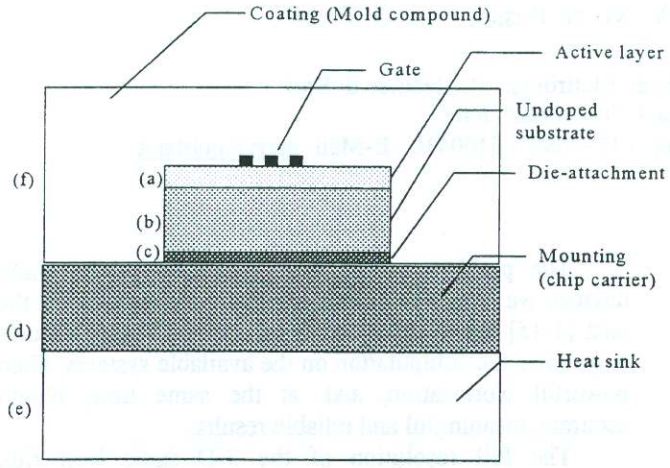

Fig. 1: Cross section of a typical GaAs chip with the top and bottom layers: n-doped GaAs active layer (a), undoped substrate (b), die attachment (c), mounting (d), heat sink (e), coating mold compound (f).

Many authors tried to solve analytically Eq. (2) and interesting solutions were obtained both with the separation technique in Cartesian or cylindrical coordinates [8-10] or the Fourier transformation of the thermal field [11].

For the time being, a full self-consistent energetic, electrical, thermal simulation for the whole multilayer structure with many transistor is so time consuming that parallel algorithms were proposed in literature to perform that task on multiprocessor systems in a reasonable time [12].

The chip package involves a great deal of problems of characterization about which interesting new papers were published in literature [13-15]. Recently, a great effort to extract a model taking into account the package has been made [13]. In this case, the difficulty in modeling a great number of transistor (i.e. heating sources) suggested the development of compact thermal models in which, with a limited number of equivalent thermal resistors connecting the channel with the external surfaces, it is possible to represent all the actual boundary condition and validate the numerical values with a database of thermal measurements.

III. THE ELECTROTHERMAL MODEL

In order to evaluate the temperature field with as much accuracy as possible, the classic and main bottom path for the heat spread has to be considered together with the top path and the natural convection of the case top surface with the still air. The feedback of the channel temperature on the drain current and a varying GaAs thermal conductivity are the physical phenomena that are to be considered in the thermal model.

A. The temperature-dependent thermal conductivity

In the multilayer structure shown in Fig.1, the thermal conductivity of the undoped GaAs substrate has the following dependence on the temperature:

$$k_{TH}(T) = \frac{A}{T^{1.2}} \qquad [W/m/K] \qquad (3)$$

in which A depends on the doping (or impurity) density, whereas all the thermal conductivity of the other layers can be considered constant with respect to T. Using the Kirchhoff transformation:

$$\Delta T_1(x,y,z) = \frac{1}{k_{TH0}} \int_{T_0}^{T_2(x,y,z)} k_{TH}(\tau)\,d\tau \qquad (4)$$

where $\Delta T_1 = T_1(x,y,z) - T_0$, $T_1(x,y,z)$ is the solution of Eq. (1) whereas $T_2(x,y,z)$ is the solution of Eq. (2), the linear Eq. (2) can be solved considering $k_{TH}(T) = k_{TH}(T_0) = k_{TH0}$ where T_0 is the temperature of the interface between the undoped GaAs substrate and the die-attachment. The reader can refer to [1] for further details on the Kirchhoff transformation.

In this way the image-problem defined by the well-known Poisson equation is solved and the actual solution of Eq. (1) is extracted through the inverse transformation.

Thus, with reference to the linearized Eq. (2), it is possible to divide the heat source, i.e. the channel of a multifinger MESFET, in suitable elementary devices as it will be detailed below. For the purpose of the present section it is important to remark that the linearity, and consequently the superposition of effects, is not applied to Eq. (1) but to Eq. (2), which is mathematically correct, whereas the solution of (2) is finally back-transformed to obtain the thermal field of the non-linear problem described by Eq. (1).

B. The solution for an elementary heat source

In order to solve the heat flux equation for a multifinger MESFET, the heat source, identified as the gate strips, has been divided into elementary square devices, each having gate length L (i.e. the same gate length of the original MESFET), and gate width L. The first step is to solve the electrothermal problem for each single elementary device (i.e. each single elementary heat source); finally the resulting thermal field of the whole structure is given by the superimposition of all the elementary fields. From a thermal point of view, the elementary heat source can be regarded as a point source corresponding, from an electrical point of view, to the elementary $L \times L$ MESFET.

It was proved that the solution of (2) for a point thermal source can be expressed as [2]:

$$\Delta T(x,y,z) = \frac{P(x_{0i}, y_{0i}, z_{0i})}{2\pi k_0 \sqrt{(x-x_{0i})^2 + (y-y_{0i})^2 + (z-z_{0i})^2}} \quad (5)$$

where (x_{0i}, y_{0i}, z_{0i}) are the coordinates of the i-th heat source, and x,y,z is the generic point in which the temperature rise $\Delta T(x,y,z)$ is evaluated, $P(x_{0i}, y_{0i}, z_{0i})$ is the dissipated power density of the i-th heat source.

C. The electrothermal feedback

Eq. (5) shows that the thermal field generated by a single heat source depends on a weighting factor $P(x_{0i}, y_{0i}, z_{0i})$, and on a geometrical factor. Each elementary thermal field can be easily evaluated from a single generic elementary field by a translation of the source center and a multiplying factor representing the power density of the specific source. The electrothermal feedback can be implemented considering that $P(x_{0i}, y_{0i}, z_{0i})$ is the electrical power density of the i-th elementary square device centered in (x_{0i}, y_{0i}, z_{0i}) and, thus, corresponding to the i-th heat source centered in the same point. The electrical power of the i-th elementary device is:

$$P(x_{0i}, y_{0i}, z_{0i}) = P(T_i(x_{0i}, y_{0i}, z_{0i})) = V_{DS} \times I_{DS}(T_i(x_{0i}, y_{0i}, z_{0i})) \quad (6)$$

where V_{DS} is the voltage drop between drain and source (considered temperature-independent) and, finally, $I_{DS}(T_i(x_{0i}, y_{0i}, z_{0i}))$ is the current of the elementary square device centered in (x_{0i}, y_{0i}, z_{0i}) having temperature T_i.

The dependence of the physical-based current-voltage equation on the temperature was widely studied in the past. For the purpose of the present paper it is important to remark that the parameters that have been taken into account for their thermal dependence are the electron mobility, the saturation velocity, the dielectric constant of the semiconductor, the energy band gap, the threshold voltage and the built-in voltage. The reader can refer to [2] for the empirical expression of the foregoing parameters.

Starting from a constant power density, corresponding for example to the power evaluated at room temperature, said z=0 the interface between the gate strips and the GaAs substrate, the thermal field in the whole semiconductor body and, most of all, in all the points $(x_{0i}, y_{0i}, 0)$, i.e. the temperature of all the elementary devices, can be evaluated, since the heat sources are supposed to be located on the chip top surface. Updating the temperature of the sources and, as a consequence, the power density, and iterating the solution of the elementary thermal fields with the corresponding weighting factors $P(T_i(x_{0i}, y_{0i}, 0))$, the temperature rise above the GaAs substrate to die-attachment interface can be calculated.

D. The multilayer structure

In order to obtain the temperature rise above the ambient, the contribution of the top and bottom layers is to be considered as it is detailed below.

With reference to Fig. 1, the bottom layers are typically a die-attachment epoxy or a metallic solder, a mounting and a heat sink. The heat sink is supposed to be isothermal and at the room temperature, the layers (c) and (d) (attachment and mounting) have constant thermal conductivity, isothermal interfaces and the contact thermal resistance is neglected. In this case the thermal resistance of these layers can be evaluated as a function of geometrical parameters [3,16] in the supplementary hypothesis of trapezoidal heat spreading with characteristic angle of 45° [16]. The thermal drop in the layers (c) and (d) is not negligible but can be well described through a one-dimensional thermal resistance.

The further step is to investigate about the effectiveness of a top path in the heat spread. Thus, a relatively low thermal resistance path (i.e. the substrate and the bottom layers) can be represented shunted with a high resistance path (i.e. the metallization, the coating layer and the natural convection between the case surface and the still air). The thermal resistance of the coating layer, typically a thick mold compound with low and constant thermal conductivity, can be evaluated under the same hypothesis of the mounting layer, i.e. as a function of the geometrical size. The ohmic contacts can be taken into account by representing the source, drain and gate metallizations as a continuous layer of metallic solder with a constant thermal conductivity (the average among those of the metals of the solder) and a constant thickness.

E. The two-dimensional I-V model

To improve the accuracy of the electrothermal model, a 2-D I-V model is to be preferred to the classic 1-D model as in the proposed simulator the computational load is not too heavy.

A physical-based 2-D I-V relation has been obtained basing on the Chang-Fetterman velocity-electric field equation [17] in which, as described in the foregoing paragraph, all the most important thermal parameters are temperature-dependent. The reader can refer to [18] for further details on the electric model.

IV. NUMERICAL RESULTS

In this Section, the presented physical-based simulator is compared with a 3-D FDM simulator [5] in order to evaluate the accuracy of the results. The calculations have been performed with reference to a MESFET with a multifinger structure having n = 28 parallel gates, each Z_u = 75 μm wide and L = 1 μm long. The distance between the sides of two neighboring gates is S = 29 μm, the GaAs chip thickness is h_S = 100 μm, the attachment layer thickness (assuming Au/Ge eutectic

metallic alloy with k_{TH} = 89 W/m/K) is h_{da} = 25 μm, the mounting layer (CM15 with k_{TH} = 182 W/m/K) is h_m = 500 μm thick. The top layers are gold metallizations (k_{TH} = 330 W/m/K, h_g = 3.5 μm), mold compound (k_{TH} = 0.2 W/m/K, h_g = 500 μm) and the natural convection between the case top surface and the still air is described by the following formula [15]:

$$R_{air} = \frac{1}{h_{nat} A_{top}} \qquad (7)$$

where R_{air} is the thermal resistance of the still air, h_{nat} = 15.5 W/m^2/K is the coefficient of natural convection, A_{top} is the case top surface. The MESFET channel aperture is W = 0.3 μm, with doping density in the active layer of N_d = $5 \cdot 10^{16}$ cm^{-3}, the heat sink temperature is T_0 = 30 °C (room temperature).

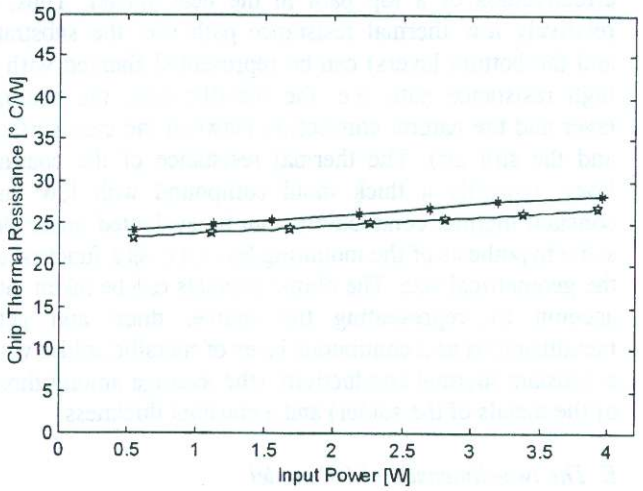

Fig. 2. Chip thermal resistance [°C/W] versus input power [W]: a comparison between the FDM simulator [3] (☆), and the proposed simulator (✳).

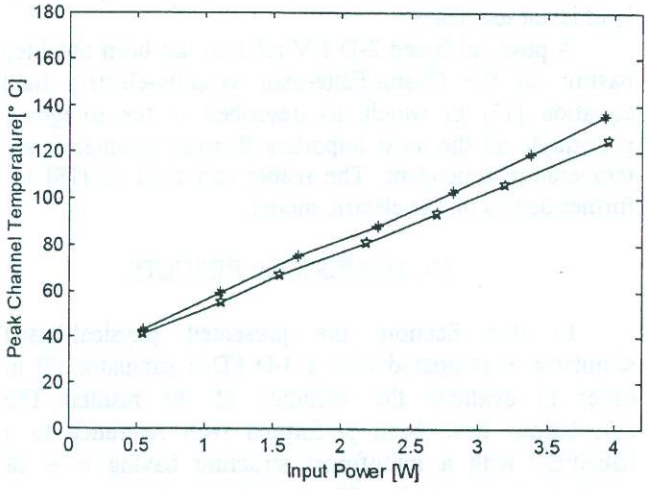

Fig. 3. Peak channel temperature [°C] versus the input power [W]: comparison between the FDM simulator [3] (☆), and the proposed simulator (✳).

Figs. 2 and 3 show the comparison between the results in terms of thermal resistance and peak channel temperature versus the effective input power P, that is the power calculated at the actual channel temperature.

The result can be considered satisfactory, especially for low input power while, for higher values of the drain current, the effectiveness in the heat spread due to the metallization, not considered in the proposed model, becomes not-negligible but produces little differences between the results.

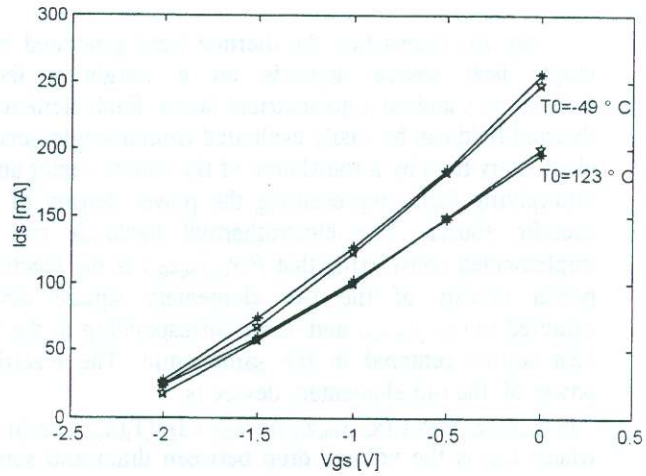

Fig. 4. Drain current [mA] versus gate voltage [V]: a comparison between the measurements (☆) and the results of the proposed simulator (✳). The device under test is a 2TX102MB MESFET produced by Alcatel and the operative conditions are T_0 = – 49 °C, and T_0 = 123 °C.

Fig. 4 shows a comparison between the measurements and results of the proposed simulator for a different multifinger device at two different ambient temperature. The device under test is a 2TX102MB produced by Alcatel. The V_{DS} has been fixed at 2.92 V and reference room-temperatures of -49 °C and 123 °C have been considered, so as to evaluate the reliability of the CAD tool in a wide range of thermal operative conditions. The agreement is to be considered satisfactory in both cases.

V. CONCLUSION

In this paper a new physical-based model for electrothermal simulation is proposed.

The light computational load and the great deal of information provided make it suitable for a PC-based implementation; the principle of resolution of the non-linear heat spread equation through Kirchhoff transformation and the discretization of the heat source, that allows the superposition of effects to be applied, can be easily extended to other analytical models in order to evaluate first the elementary thermal fields and then the resulting global effect of one or more active device (MESFETs, HEMTs, HBT, SOI MOSFETs, lasers). Here an example with a possible analytical solution for a point

source is given. The comparison with a FDM simulator and some measurements is to be considered satisfactory.

A suitable trade-off between accuracy and quantity of produced results and computational load has been reached on a common PC.

VI. REFERENCES

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