# Modelling of a 4-18GHz 6W Flip-Chip Integrated Power Amplifier based on GaN HEMTs Technology

Sandra De Meyer[1], Audrey Philippon[1], Michel Campovecchio[1], Christophe Charbonniaud[1], Stéphane Piotrowicz[2], Didier Floriot[2], Raymond Quéré[1]

[1]IRCOM-MITIC, CNRS UMR 6615, 123 Avenue A. Thomas, 87000 Limoges, France, (33)5-55-45-77-34
[2]Thalès-TRT-MITIC, Domaine de Corbeville, 91404 Orsay Cedex, France, (33)1-69-33-92-44

*Abstract* — **This paper reports on the design of a cascode GaN HEMT distributed power amplifier demonstrating significant improvement of the best power performances reported to date. The active device is a 8x50µm AlGaN/GaN HEMT grown on siSiC. The distributed power amplifier integrates 4 cascode cells capacitively coupled to the gate line for power optimization. The active part made of the 4 cascode cells is implanted on a GaN-based wafer while the distributed passive part made of the interconnection lines is implanted on an AlN substrate. Finally, the GaN-based wafer integrating the active part is flip-chipped onto the AlN substrate via electrical and mechanical bumps. The flip-chip integrated circuit demonstrates a mean gain of 10dB and input/output matching lower than –10dB over the 4-18GHz bandwidth. At an input power of 29dBm (1db comp.), power simulations exhibit a mean output power of 37.6dBm with a standard deviation of 0.3dB, a power gain of 8.6dB and 16% of PAE over the band. At an input power of 31dBm (2dB comp.), the distributed amplifier achieves a mean output power of 38.6dBm, a power gain of 7.6dB and 18% of PAE.**

## I. Introduction

The wide band-gap materials have focused the researchers attention these last years due to their ability to operate at high frequencies and high temperatures as well as their performances demonstrated for high power applications [1]. The gallium nitride growth process has been considerably improved lately allowing to get higher power densities from a single transistor [2]. The AlGaN/GaN based high electron mobility transistors (HEMTs) are promising candidates for high-power wideband solid-state amplifiers [3]-[4]. As GaN wafers remain rare, in small dimensions and anyway very expensive, most of the devices are developed on other materials such as silicon (Si), silicon carbide (SiC) or single-crystal sapphire ($Al_2O_3$). The best power performances have been demonstrated on SiC substrates, mainly due to its higher thermal conductivity and better crystallographic match with the GaN material. Considering the high objectives in terms of power level, a strong attention needs to be observed regarding the thermal management. A flip-chip mounting has been considered in this study onto an aluminum nitride substrate (AlN) presenting a high thermal conductivity.

## II. GaN Technology

In this study, the device considered is a coplanar AlGaN/GaN HEMT processed on a silicon carbide wafer on which a thin film of gallium nitride has been grown by metal organic chemical vapor deposition (MOCVD) technique. The active device used in the design is a 400µm HEMT (8x50µm) of 0.15µm gate length. Pulsed I-V characteristics and S-parameters measurements have been performed on several devices to derive the non linear models for power amplifier design [5].

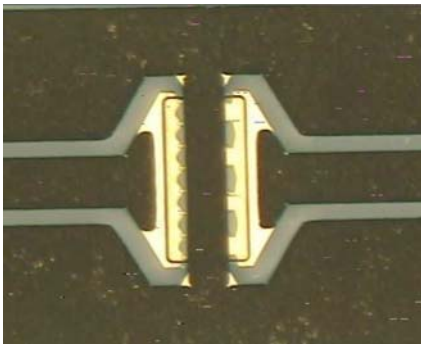

Fig. 1. Photograph of a 0.15µm gate length and 400µm gate width AlGaN/GaN HEMT (8x50µm).

The non-linear model is based on modified Tajima equations and splines. This model integrates two source accesses because the grounding of transistors was performed through vias on the AlN substrate on both side of the source air-bridge. These models have been implemented in a commercial simulation environment in order to design the distributed power amplifier.

## III. Design of the Amplifier

The power amplifier is an optimized distributed architecture integrating capacitively coupled gate line and power optimized cascode cells. Fig. 2 shows the general schematic of the distributed power amplifier. Such a topology is known to be very efficient for wideband power optimization[6]. It should be noticed that the specific design procedure of such a distributed architecture [7] requires first to optimize the power performance of the cascode cell fixing the power matching between transistors through an additional capacitor *Ca* placed on the gate of the common gate transistor. Then, the final optimization goals of the passive distributed architecture take into account the power load requirements of each cascode cell within the distributed amplifier in order to not only ensure wideband gain and matching but also wideband power performances.

Due to the high power levels brought into play in this project, a close attention must be paid to the thermal management because of the relatively high dissipation needed to avoid any circuit failure. Moreover, via-holes could not be realized onto the GaN substrate so that the grounding had to be done an other way. For these reasons, the flip-chip mounting onto a good-thermal-conductivity material has been considered. The material used for the flip-chip report is aluminum nitride (AlN), presenting a good thermal conductivity (180 $W.m^{-1}.K^{-1}$). The mechanical and electrical contacts are ensured by Sn/Au bumps. Finally, the active cascode cells and their matching networks (*Ca, Cg, Rp*) were designed on the gallium nitride wafer while the input/output gate and drain lines and the DC-bias paths were realized on the aluminum nitride substrate.

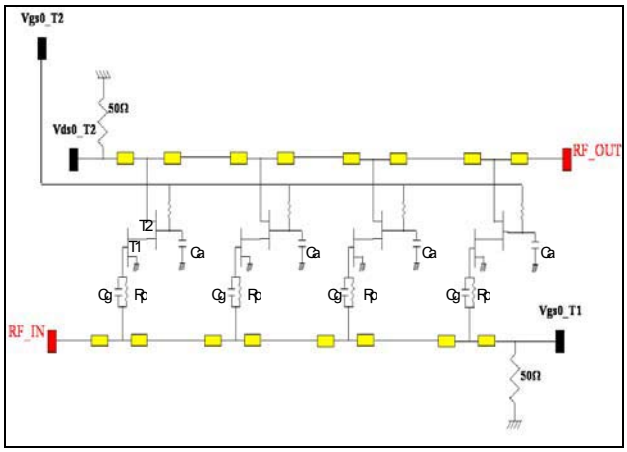


Fig. 2. General schematic of the capacitively coupled distributed amplifier integrating optimized cascode cells.

*A. GaN design (active part)*

The optimum number of cells to consider in the distributed structure has been determined with the help of an analytical design rule (1) where $\alpha_g$ and $\alpha_d$ are the frequency dependent attenuations of the artificial gate and drain line sections including the intrinsic elements of transistors.

$$N_{opt}(\omega) = \frac{\ln(\alpha_d) - \ln(\alpha_g)}{\alpha_d - \alpha_g} \qquad (1)$$

Considering that the final cascode configuration can be considered as a single transistor showing a lower input capacitance and a higher output impedance, the optimum number $N_{opt}$ determined that way for the 8x50µm GaN HEMT is equal to 4 cascode cells.

The Fig. 3 shows the layout of the distributed active structure integrating the four cascode cells designed on the GaN substrate. The dimensions of the GaN chip is less than (3.5x1.1)mm².

For better power transfer from the transistor T1 (1st transistor of the cascode cell) to the transistor T2 (2nd transistor of the cascode cell), the drain pad of T1 is connected to both part of the source metallization of T2. Transistors T1 are grounded on the AlN substrate through their air-bridge playing the role of an electrical bump.

For optimized power matching of the cascode cell, series MIM capacitor *Cg* are integrated on the GaN to couple the cascode cells to the gate line (Fig. 2). This capacitor enables to lower the input equivalent capacitance of the active cells inducing an easier power matching within the distributed architecture up to the maximum frequency of the bandwidth. Large resistors *Rp* are integrated in parallel to those capacitors to realize the gate bias path noticing that there is no gate current flowing through the transistors

.

When optimized, the cascode configuration enables to ideally sum the output voltage of each transistor so that we obtain twice the output power of a single transistor. Indeed, a classical cascode cell does not meet these conditions because the 2nd transistor input limits the output voltage of the 1st transistor. To solve this problem, an additional capacitor *Ca* must be placed in series with the gate of the common gate transistor T2 in order to implement a frequency independent tension divider between *Ca* and the input capacitance *Cgs* of the 2nd transistor. This capacitor value is optimized under large signal conditions (non-linear simulation of the cascode cell close to 1dB compression) to synthesize the required tension ratio between the optimum large signal control voltages Vds(T1) and Vgs(T2).

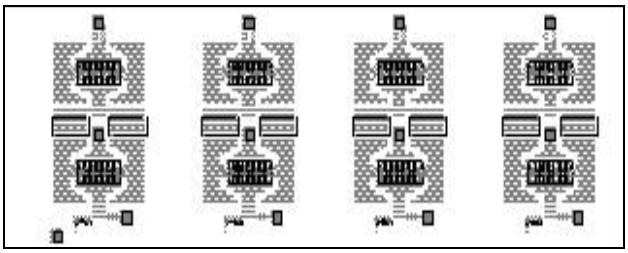

Fig. 3. Layout of the distributed topology based on four cascode cells designed on the gallium nitride material.

*B. AlN design (passive part)*

The design on the AlN wafer integrates the gate and drain lines as well as the gate and drain terminations. The RF/DC decoupling circuits are also included onto the AlN material allowing to get an integrated amplifier. The Fig. 4 shows the layout of the passive circuit realized on the aluminum nitride. It presents five access pads : the RF input and output pads, the gate bias pads of T1s and T2s and the drain bias pad of the cascode cells. Notice that the value of this last DC voltage has to be twice the bias level of a single transistor. Each bias line integrates small and large MIM capacitors coupled to ground in order to ensure high and low-frequency decoupling.

The AlN design also integrates all the via-holes that permit to ground the transistors. The gate and drain loads of the input and output lines have been fixed to 50 ohms. The dimensions of the AlN chip are less than (9x6)mm².

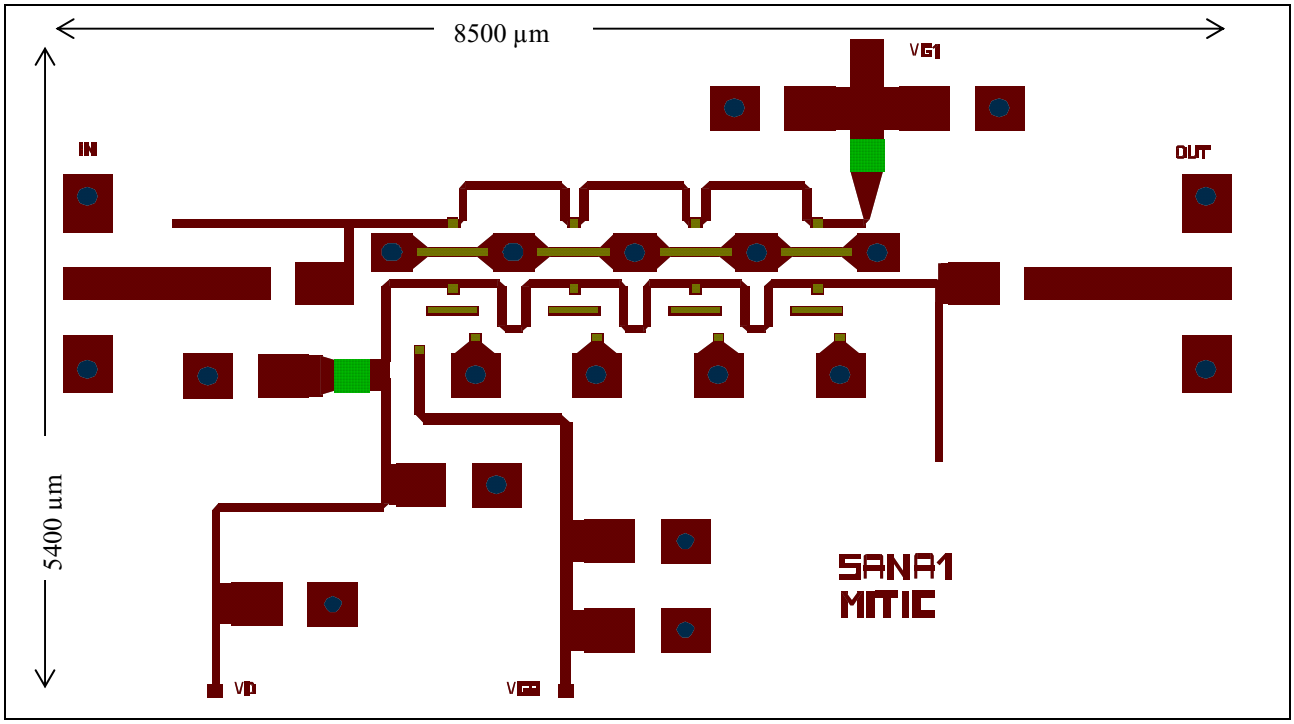


Fig. 4. Layout of the input an output lines as well as the DC bias lines and their RF/DC decoupling components.

## IV. Simulation results

The design of the amplifier has been performed with the help of the ADS simulation software. In order to ensure valid results, hybrid simulations have been performed using electrical and electromagnetic analyses. The structure has been first optimized through non-linear circuit simulations while the resulting layout obtained has been electromagnetically analyzed to check for any parasitic coupling effect and correct it.

Linear simulations show 10dB average gain over the 4-18GHz band with associated input and output matching lower than –10dB up to 21GHz.

Active cascode cells are known to be very prone to oscillations so that the amplifier stability is one of the most important design issue. The Rollett factor and the stability measure parameters have been used to ensure the circuit stability during the design process. Moreover, an additional stability analysis has been implementing using the normalized determinant function (NDF) to check the intrinsic stability of each active device within the distributed amplifier. To implement such a necessary stability analysis, the electrical device models are modified to enable the open loop analysis[8].

For power operation, transistors are biased at -6V gate voltage and 20V drain voltage corresponding to Idss/3.

The Fig. 5 presents the evolution of output power, gain and PAE versus input power at mid-band (12GHz). We can observe a low level power gain of 9.5dB up to 25dBm input power. At -1dB (29dBm input power), we notice an output power of 37.4dB (5.5W) and 15% PAE. At -2dB (31dBm input power), the amplifier can achieve 38.5dBm output power (7.1W) and 16.4% PAE.

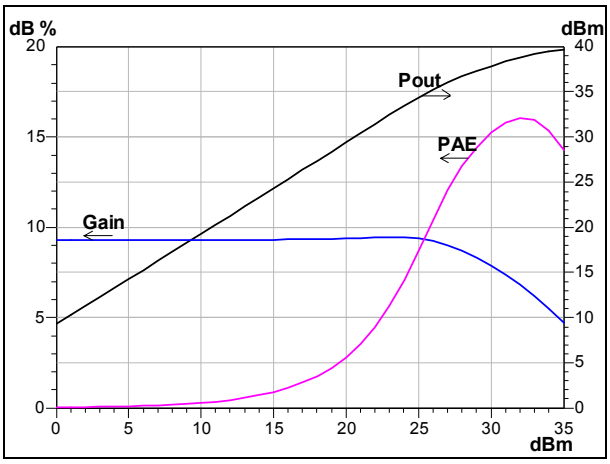


Fig. 5 Graphs of output power, power gain and PAE versus input power in dBm at 12GHz.

The Fig. 6 presents the evolution of input/ouput matching and output power versus frequency at -1dB and -2dB. At 29dBm input power (-1dB), the amplifier exhibits a mean output power of 37.6dBm (5.8W) over the 4-18GHz band associated to a mean value of 16% PAE and a flat power gain of 8.6dB. At -2dB (31dBm input power), the amplifier exhibits a mean output power of 38.6dBm (7.2W) over the 4-18GHz band associated to a mean value of 18% PAE.

Talking about thermal issues, a quick calculation has been made to check the maximum dissipated power the transistors could accept. The termal resistance of a 8x125µm parallel device has been determined to be 14.1°C/W. By scaling, we could defined the thermal

resistance of a 8x50µm device at 35.25°C/W. Considering a maximum junction temperature of the active devices of 200°C, we could accept a dissipated power of 5.7W from each transistors.

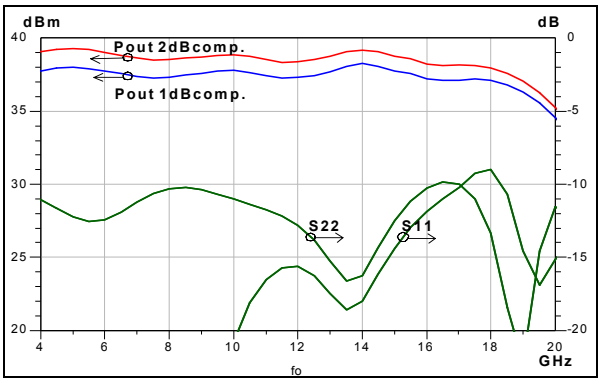


Fig. 6 Input/Output matching and output power @1dB and 2dB compression versus frequency.

Simulation results of dissipated power of each active device for 29 and 31 dBm input power (respectively 1 and 2dB compression) show a maximum dissipated power of 5.6 W concerning the second transistor of the first cascode cell. This means that the amplifier may be measured under CW conditions until 2dB compression. But these results are only simulated results and even though the value is extremely close to the limit of 5.7W. For these reason, the amplifier should be measured under pulsed conditions to avoid any thermal induced failure of the active devices.

We have exposed the simulated power results obtained from a cascode distributed amplifier based on 8x50µm GaN HEMTs. Another circuit, implementing the same distributed topology has been designed using 8x75µm transistors of the same AlGaN/GaN technology. Simulated results of this 2nd circuit present higher output power levels but less flat. Test cells were designed in order to check the performances of a single cascode cell. Active part on GaN is assembled like previously on AlN by flip-chip report for biasing, via-holes and thermal management. As cascode cells are prone to oscillations, two versions are designed : one with resistance of stability at the gate of the transistor T2, the other without. Both GaN chips are being realized as well as both AlN chips optimized for each GaN design.

## V. Conclusion

For the first time, a power distributed amplifier based on cascode AlGaN/GaN HEMTs has been designed using flip-chip technology on AlN substrate. The circuit architecture implements capacitive gate coupling on the gate line and power optimized cascode cells to obtain 10dB linear power gain and 6W output power at 1dB compression over the 4-18GHz bandwidth. These simulation results are very promising ; realization of both GaN MIC and AlN carrier are in progress.

## ACKNOWLEDGEMENT

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## References

[1] R. Coffie & al., "Unpassivated p-GaN/AlGaN/GaN HEMTs with 7.1W/mm at 10GHz," *Electronics Letters, vol. 39, pp. 1419-1420,* Sept. 2003.

[2] K.K. Chu & al., "9.4-W/mm power density AlGaN-GaN HEMTs on free-standing GaN substrates," *Electronics Device Letters, vol. 25, pp. 596-598,* Sept. 2004.

[3] J.J. Xu & al., "A 3-10GHz Ga-N based flip-chip integrated broad band power amplifier," *IEEE Transactions on MTT, vol. 48, pp. 2573-2577,* Dec. 2000.

[4] R. Behtash & al., "Coplanar AlGaN/GaN HEMT power amplifier MMIC at X-band," *IEEE MTTS Digest, pp. 1657-1659,* June 2004.

[5] C. Charbonniaud & al., "Power performance evaluation of AlGaN/GaN HEMTs through Load-pull and Pulsed I-V Measurements," *12th International GaAs Symposium, pp. 163-166,* 2004.

[6] C. Duperrier & al, "New design method of Non-Uniform Distributed power amplifiers. Application to a single stage 1W PHEMT MMIC" *IEEE Transactions on MTT, vol.49,pp. 2494-2500, Dec.2001.*

[7] J.P. Fraysse & al., "A 2W high efficiency 2-8GHz cascode HBT MMIC power distributed amplifier," *IEEE MTTS digest, vol. 1, pp. 529-532,* June. 2000.

[8] M. Campovecchio & al, "Stability analysis of millimeter-wave circuits. Application to DC-40GHz PHEMT amplifier and Ku-band HBT power amplifier", *30th European Microwave Conference, vol. 2, pp. 294-297, Oct. 2000.*