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# A Low-Power GaAs Flip-Flop

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**Abstract** : This paper describes a low-power high speed flip-flop in Gallium Arsenide (GaAs) called PCLF for Pseudo-Complementary Logic Flip-Flop. The PCLF offers attractive power saving without performance degradation and is fully compatible with existing FET logic families. It can be efficiently used in the VLSI ICs, as well as in multigabit/second SSI or MSI ICs. As an example a D-flip-flop, T-flip-flop and a 1/8 divider have been designed and fabricated, verifying the expected low power dissipation.

## 1. INTRODUCTION

Gallium Arsenide (GaAs) technology has demonstrated characteristics which make it highly suitable for high performance high speed systems.
However, the high-power dissipation per gate as well as the low thermal conductivity of GaAs prevent the realization of real VLSI systems on this material.
Thus, the existence of VLSI circuits in GaAs depends on the avaibility of low-power: Logic family, Macocells and Flip-Flop (register).
Recently, a lot of effort has been spent in the development of low-power logic families. One can mention the dynamic logic TDFL (Two-phase Dynamic FET Logic) [1], which presents a very-low power consumption. More recently, a static family, PCFL (Pseudo-Complementary FET Logic) [2] was described, which consumes slightly more than TDFL, but do not need any clock. These two approaches are good candidates to the realization of VLSI systems on GaAs.
Direct Coupled FET Logic (DCFL) (Fig. 1), which looks like NMOS logic in Silicon, is the most compact and widely used logic family in GaAs because of its simplicity [3] [4]. Up to now GaAs flip-flops were designed with DCFL gates. Apart from its high power dissipation, the conventional DCFL flip-flop needs more than four gates on the critical path (Fig. 2), which limits its high speed operation.

To overcome the problem of the delay time in the DCFL flip-flops and to enhance the DCFL simplicity advantage, a DCFL Memory Cell Flip Flop (MCFF) has been proposed [5] [6]. The MCFF (Fig. 3), designed with an advanced GaAs HEMT technology, has a master-slave configuration and is composed of transmission gates, DCFL memory cells and buffers. The MCFF is especially applied to multigigabit/second SSI or MSI because of its high speed operation. However, the high power consumption of the DCFL and Memory Cell Flip-Flop prevents their use in complex high speed systems.

This work aims to design a flip-flop for the GaAs VLSI application using conventional process and reaching the following features:

- High speed operation
- Simple topology
- Low power dissipation.

## 2. CIRCUIT TECHNIQUE

Pseudo-complementary FET logic (PCFL) has been demonstrated to be a very low-power static logic family in GaAs [2]. Moreover, the PCFL gates are fully compatible with existing FET logic families, namely DCFL and TDFL.
This logic family uses complementary signals, and it is composed of two types of gates: PCFL1 and PCFL2 (Fig. 4, 5). PCFL1 gates have a very low power consumption, but suffer from a level degradation at high speed. PCFL2 gates compensate the level degradation by using a bootstrapping technique. The price to be paid is a slightly higher power consumption and a higher complexity.

It has been shown in [2] that the output level degradation in the PCFL1 will be reduced when the supply voltage is increased, at Vdd=2V there is no degradation at all.

A new flip-flop using PCFL gates with low-power dissipation has been designed. This flip-flop is called PCLF for Pseudo-Complementary Logic Flip-Flop, it has the same structure as the original Memory Cell Flip-Flop (MCFF) [3] (Fig. 3, Fig. 7).

Like MCFF, PCLF operates as follows:

When $Clk$ is high, the transmission gates of the master latch J1 and J2 are ON, the complementary data signals $D$ and $\bar{D}$ are written in the master memory cell. In the same periode, $\overline{Clk}$ is low , the transmission gates of the slave latch J3 and J4 are OFF, the slave memory cell is isolated from the master latch, therefore outputs levels of $Q$ and $\bar{Q}$ are kept constant. When $Clk$ is low, the transmission gates of the master latch J1 and J2 are OFF, the master memory cell is isolated from $D$ or $\bar{D}$, therefore the output levels of the driving inverters of the

master latch are kept constant. In the same period, *Clk* is high, the transmission gates of the slave latch J3 and J4 are ON, the output levels of the driving inverters of the master latch are written in the slave memory cell through the transmission gates in parallel with setting up $Q$ and $\overline{Q}$.

In the original Memory Cell Flip-Flop, the memory cell of the master and slave latches is composed of cross-coupled DCFL inverters. It operates in the same way as in a static RAM. The structure of the whole MCFF is fully differential, thus it is well adapted to the use of PCFL logic.
Another important advantage of a differential operation is the good noise immunity.
The transmission gates are realized using enhancement transistors and, as the accesses of the memory cell are at low impedance levels, the pass transistors do not need special care to reduce their leakage currents when they are in the off state. Concequently, the voltage levels of the clocks are the same as any other signal in the circuit.
To reduce the power dissipation of the flip-flop without degrading the speed, the original MCFF has been modified in the following way:

-the memory cells are designed using the PCFL1 inverters (Fig. 8). Like CMOS, PCFL1 gates consume only dynamic and short-circuit power, with the distinctive feature that the dynamic power in PCFL1 is very small thanks to the small swing (typically 0.6V) and the reduced parasitic capacitances. When compared to the DCFL version of MCFF, the use of the PCFL1 in the design of the memory cells eliminates static power dissipation which vary from 0.5 to 1.0 mW/gate in DCFL, depending on the speed. Furthermore, in a DCFL memory cell, both inverters always consume a static current.

## 3. EXPERIMANTAL RESULTS

A test circuit has been integrated using the Vitesse H-GaAs III process, which features 0.6µm long MESFETs [7]. The circuit includes the already mentioned PCLF D-flip-flop (D-FF), a T-flip-flop (T-FF) and a 1/8 divider. The schematic diagram of the 1/8 divider is shown in Fig.9. Fig. 10 is a micrograph of the die. In this IC, DCFL input amplifiers are introduced to obtain the complementary inputs for both the data ($D$ and $\overline{D}$)and the clock ($Clk$ and $\overline{Clk}$).
Shown in Fig. 11 and Fig. 12 are respectively measured input and output waveforms of the D-FF and T-FF at a clock frquency of 500MHz with 2V supply.
The measured complementary outputs of the 1/8 divider at a clock frquency of 900MHz with 2V supply are shown in Fig. 13.
Table I summarizes the experimental results.

Table I:
Experimental results

| Circuit | I (mA) (Simulation) | I (mA) (Experimental) |
|---|---|---|
| D-Flip-Flop (DCFL) | 2.37 | / |
| D-Flip-Flop (PCLF) | 1.1 | 1.3 |
| T-Flip-Flop (PCLF) | 1.3 | 1.4 |
| 1/8 Divider (PCLF) | 3.38 | 3.6 |

We can see from the table I that the power dissipation of the PCLF has been reduced by 50% compared to the conventional DCFL flip-flop.

Further refinement of the PCLF is shown in Fig. 14. This circuit has the best power performance than the circuit shown in Fig. 3. The improvement is obtained by replacing the two DCFL output buffers in the master and in the slave latches by PCFL2 inverters.

Although PCFL1 inverters are slower than DCFL ones, they are used for storage operation, where consumption is important and speed is not. On the other hand, PCFL2 inverters are used where speed is needed.

Fig. 15 shows the dependence of the maximum operating frequency and the power consumption of the PCLF (Fig.14) with the supply voltage. At 2V supply, the power dissipation of the PCLF is 1.1 mW, while the maximum clock frequency reaches 8GHz.
Fig. 16 shows a comparison at 8GHz between a PCLF and other flip-flops. The power consumption of PCLF is reduced by 76% and 60% compared to the conventional DCFL flip-flop and MCFF.

Furthermore the ratio of the threshold voltage variation to the noise margin is critical to determining the IC electrical yield [8]. And as the PCFL gate uses enhancement type MESFETs (EMESFET) only, its sensivity to process variations is lower than DCFL. This is due to the generally larger process spreads of depletion type transistors. Thus, the acceptable PCLF noise margin, and the less sensitivity to threshold variation result in larger functional yield.

## 4. CONCLUSION

A new GaAs flip-flop based on the PCFL logic family has been proposed. While being able to be clocked at high speed, the Pseudo Complementary Logic Flip-flop is an attractive solution to save power consumption. Thus the PCLF is a promising candidate for low-power high speed GaAs digital applications.

## 5. REFERENCES


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[8] S. I. Long and M. Sundaram, "Noise-Margin Limitations on Gallium-Arsenide VLSI," *IEEE J. Solid State Circuits*, vol. 23, pp. 893-900. Aug. 1988.


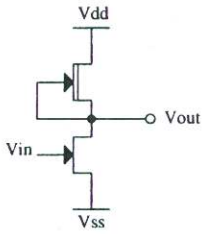


Fig.1 DCFL gate inverter.

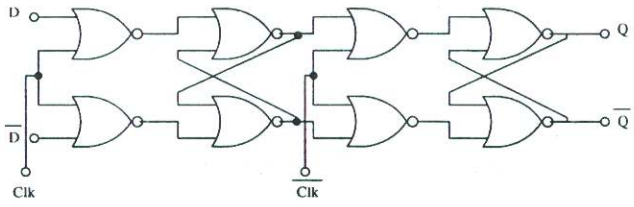


Fig. 2 Conventional DCFL flip-flop.

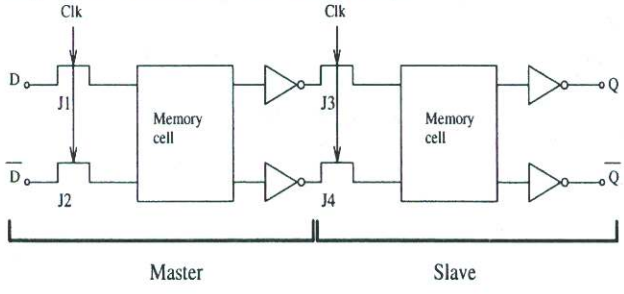


Fig. 3 Memory Cell Flip-Flop (MCFF).

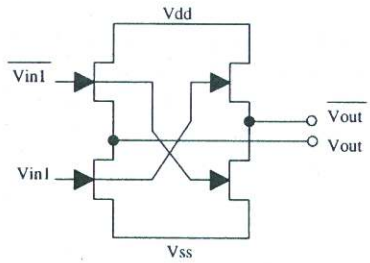


Fig. 4 PCFL1 inverter.

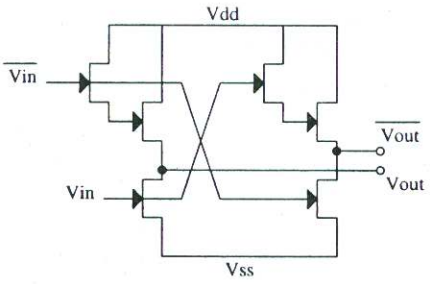


Fig. 5 PCFL2 inverter.

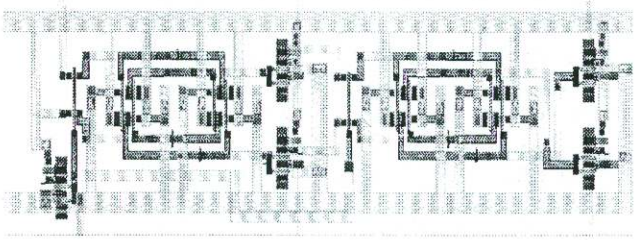

Fig. 7 Layout of a PCLF. Cell dimensions are 250μm X 70μm.

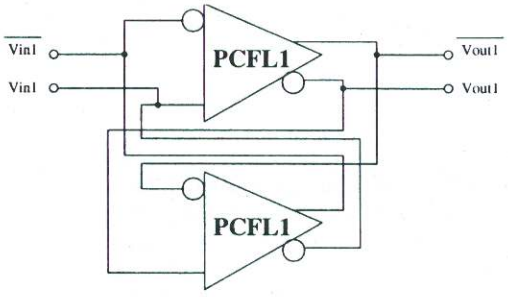


Fig. 8 PCFL1 memory cell.

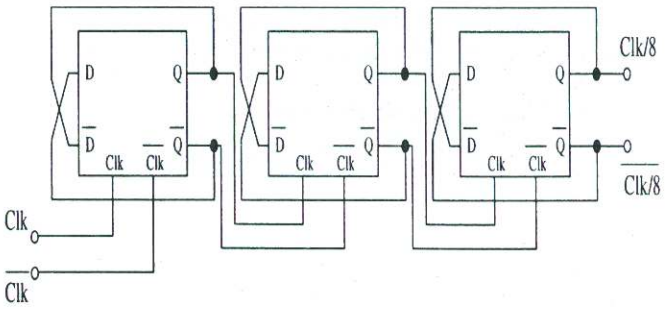


Fig. 9 Schematic diagram of the 1/8 divider.

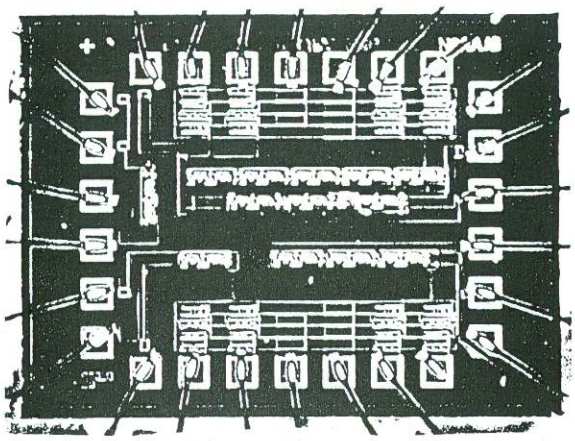

Fig.10 Die photograph.

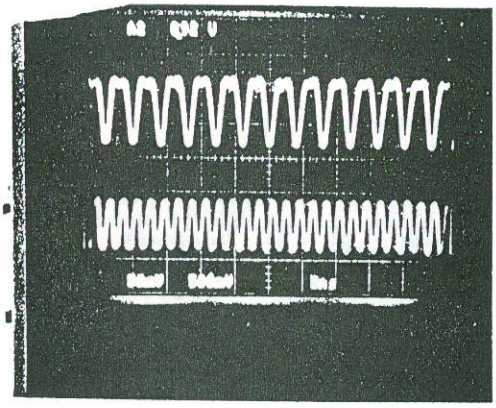

Fig.11 Measured input and output waveforms of the D-FF at 500MHz clock frequency.

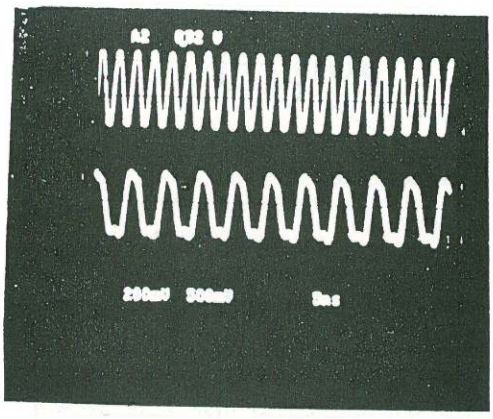

Fig.12 Measured input and output waveforms of the T-FF at 500MHz clock frequency.

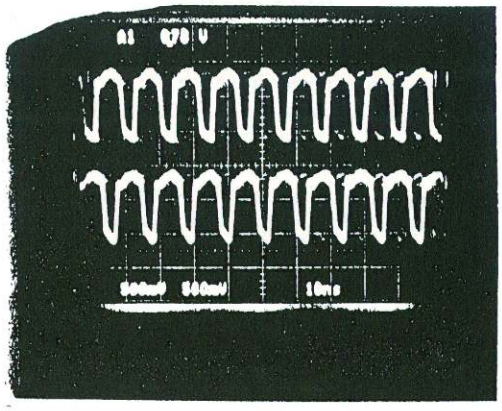

Fig.13 Measured complementary output waveforms of the 1/8 Divider at 900MHz clock frequency.

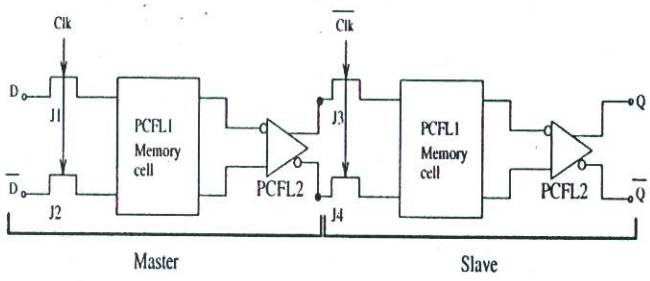


Fig. 14 Schematic diagram of the PCLF.

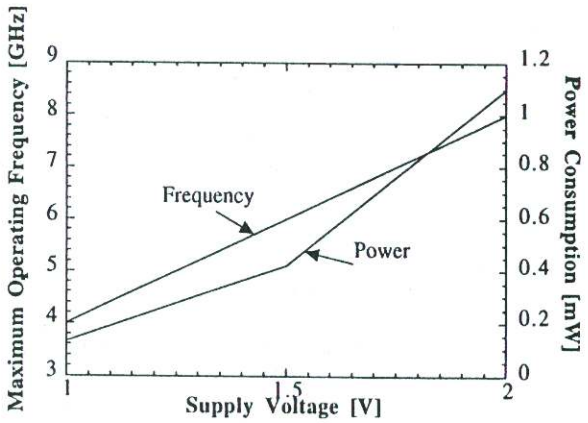


Fig. 15 Simulated operating speed and the power consumption of the PCLF.

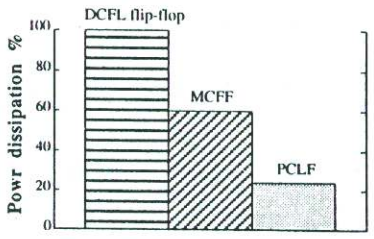


Fig. 16 Power dissipation comparison at 8GHz clock frequency.