GAAS® 97 • 5th European Gallium Arsenide and related III-V compounds Applications Symposium
Bologna, Italy - September 3rd-5th, 1997

DC, RF and Low Frequency Noise Characterization of C and In/C doped GaInP/GaAs HBT's

M. Borgarino*, R. Plana†, L. Escotte†, S. Delage‡, H. Blanck‡, F. Fantini *, J. Graffeuil †

* Dipartimento di Ingegneria dell'Informazione, Università di Parma, Viale delle Scienze, 43100 Parma, Italy

† Laboratoire d'Analyse et d'Architecture des Systemes - CNRS, 7, Av. Colonel Roche, 31077 Toulouse Cx, France

‡ Thomson LCR Domaine de Corbeille, 91404 Orsay Cx, France

Abstract

This paper presents a comparative study, based on DC, RF and low frequency noise (LFN) measurements, between Carbon-doped, and Indium/Carbon doped GaInP/GaAs HBT's featuring different emitter widths. Both technologies exhibit an evident emitter size effect, while C-doped devices have larger DC and RF gains and a lower input voltage noise level. The better performance has been justified in terms of a higher quality of the extrinsic base surface. This explanation was supported by the LFN measurements carried out on self-aligned devices, which revealed an electron diffusion current from the emitter toward the base, probably due to the pinning of the Fermi level at the surface. The HBT's have been compared also in terms of reliability by means of electrical stress performed at room temperature. The effect of the stress was a DC current gain increase associated with a reduction of the base current and of the input voltage noise lorentzian component. The In/C doped devices exhibited the largest variations, and were more sensitive to the current stress.

1 Introduction

The GaInP/GaAs HBT is a very interesting and promising device both for digital [1], microwave [2] and low power [3] applications.
Nevertheless, some problems are still present in the today GaInP/GaAs HBT's technology.
From the low frequency noise point of view, the excess noise in GaInP/GaAs HBT's must still be minimized [4], even if the absence of Aluminium, of DX centers and the low surface recombination velocity offer advantages over AlGaAs/GaAs HBT's.
Moreover, the high level of Carbon concentration in the base induces a lattice shrinkage, which can negatively impact the reliability [5]. Data reported in the literature suggest that the Indium codoping can reduce the lattice shrinkage and improve the device reliability [6].
The emitter scaling down has to be taken into account also, because the *emitter-size* effect [7] can seriously degrade the device performance.
In the present work we report a comparative study, based on DC, RF and LFN measurements between C and In/C doped GaInP/GaAs HBT's featuring the same emitter length (L_E) but different emitter width (W_E). Eventually, the two types have been compared also in terms of reliability by means of a DC stress.

2 Experimental

The epitaxial structure of the investigated HBT's is reported in Table I. The wafers are MOCVD grown and

	Layer	Thickness(μm)	Doping(cm^{-3})
7	GaAs:Si	0.20	$n=3.1*10^{18}$
6	GaInP:Si	0.10	$n=9.1*10^{17}$
5	GaInP:Si	0.25	$n=1.2*10^{17}$
4	GaInP:Si	0.15	$n=3.1*10^{17}$
3	GaAs:C	0.12	$p=5.0*10^{19}$
2	GaAs:Si	1.00	$n=1.5*10^{16}$
1	GaAs:Si	0.80	$n=3.1*10^{18}$
	SI GaAs Substrate		

Table 1: Epitaxial structure of the HBT's under test.

the devices are double mesa processed and SiN passivated. In the following we will refer to the convential C-doped HBT's as type A and to the Indium codoped HBT's as type B. The devices have been stressed in the forward active region at room temperature by applying a collector emitter voltage V_{CE}=7.65V and by forcing a collector current density between $1 \cdot 10^3 A/cm^2$ and $1 \cdot 10^4 A/cm^2$. All characterizations and stresses have been carried out at wafer level.

3 Results and Discussion

Fig. 1 reports the comparison between Gummel plots of type A HBT's featuring different emitter widths. The currents were normalized in order to compare the base currents at the same collector current. The transistors featuring the largest emitter width exhibit the lowest base current; the same conclusion can be drawn for type B HBT's (Fig. 2). It is interesting to compare the Gummel plots of HBT's of different base doping. Fig. 3 depicts the comparison carried out for W_E=3μm. After normalizing the currents, we can observe that there is no difference in the base currents. The same comparison performed for W_E=1μm shows that the type B transistors exhibit a larger base current (Fig. 4).

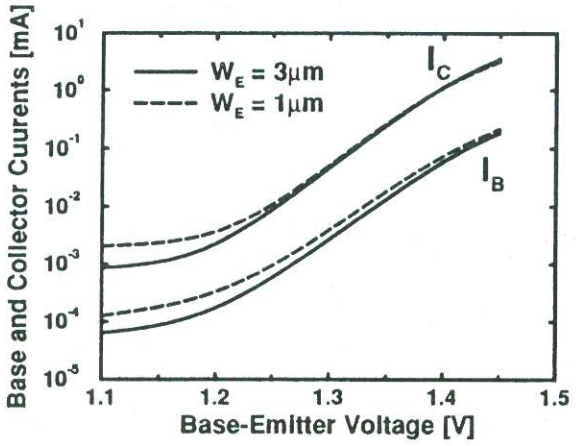

Figure 1: Gummel plots of type A HBT's.

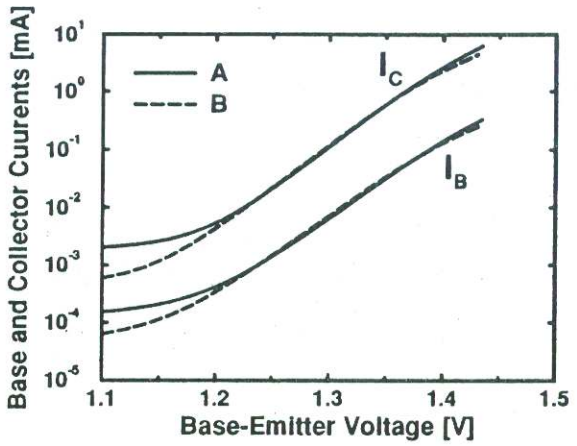

Figure 3: Gummel plots for HBT's with W_E=3μm.

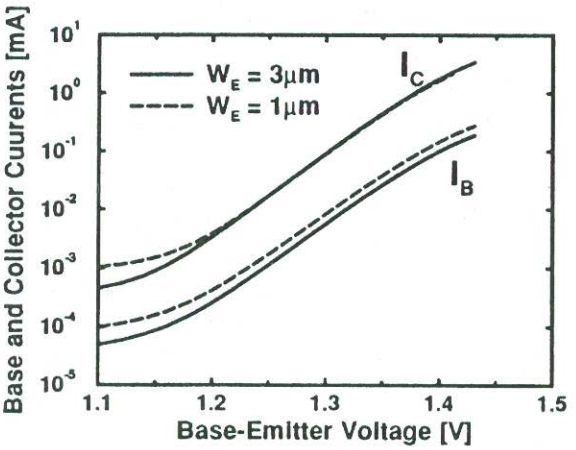

Figure 2: Gummel plots of type B HBT's.

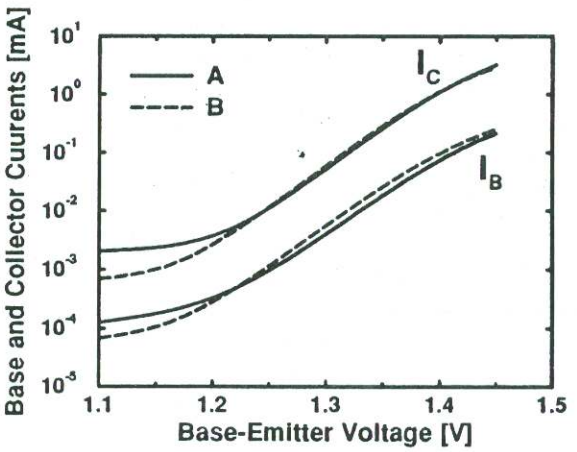

Figure 4: Gummel plots for HBT's with W_E=1μm.

The Gummel plots indicate that the base current increases when reducing the emitter width, for both transistor types, independently of the Indium presence in the base layer. These results are mirrored by the DC current gain β (Fig. 5). For the same W_E, the difference between the β values is larger for the HBT's with the smallest emitter width. A larger reduction of β for the smallest devices suggests a surface recombination mechanism. This is confirmed by the presence of a pronounced emitter-size effect (Fig. 6). From the line slopes, we can compute the extrinsic base surface recombination current divided by the emitter length (K_{surf}) [8]. In agreement with the previous results, we found that type A devices exhibit a lower value of K_{surf}.

Fig. 7 compares the input voltage noise spectra for devices of the two technologies, featuring different emitter widths. All the spectra show a large lorentzian component in the 1kHz-100kHz frequency range. For both types, we can observe that the transistors with the smallest W_E exhibit the highest lorentzian component. For the same W_E, the type B devices exhibit a higher noise level. These results indicate that the recombination mechanisms are more effective in the type B, in agreement with the considerations carried out from DC measurements.

Both DC and LFN measurements, therefore, confirm that the difference between the two technologies is related to surface effects, which affect also the high frequency performance, as shown in Fig. 8. The transistors featuring W_E=3μm exhibit a larger RF gain at frequency below about 3Ghz in agreement with the behaviour of DC static gains (Fig. 5). At frequencies higher than 5Ghz, the HBT's with W_E=1μm exhibit a larger $|S_{21}|$, probably thanks to the smaller parasitic capacitances.

In order to complete the comparison, we carried out extra DC, RF and LFN measurements on self-aligned transistors. The most interesting result concerns the low frequency noise characterization. In particular, the input current noise spectra of self-aligned devices exhibit a much higher 1/f component (Fig. 9). This can be explained by taking into account the pinning of the Fermi level at the base-emitter junction. According to the work of Tiwari and Frank [9], the Fermi level pinning at the base-emitter junction allows some electrons injected from the emitter into the base to flow towards the extrinsic base surface. Since for self-aligned devices the distance between base and emitter contacts is very small, this diffusion current gives rise to a typical 1/f noise component. For the devices that are not self-aligned, the diffusion current gives rise to a large recombination current at the extrinsic base surface. Therefore, the 1/f noise component further

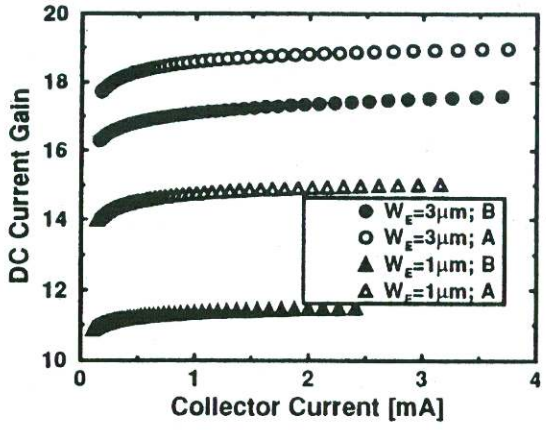

Figure 5: DC current gains versus collector current.

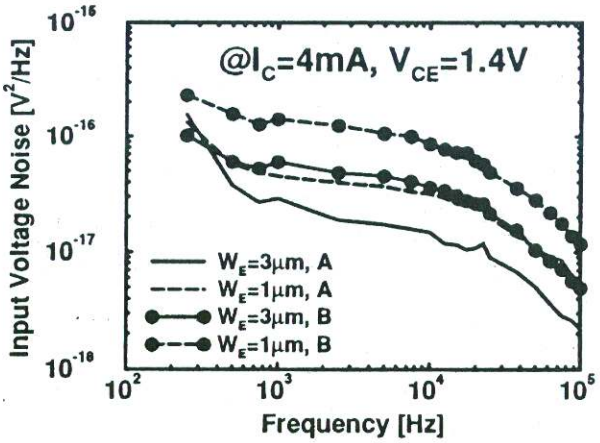

Figure 7: Input voltage noise.

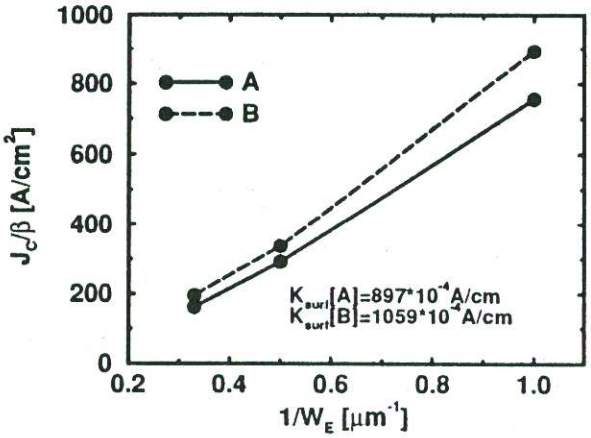

Figure 6: Emitter size effect.

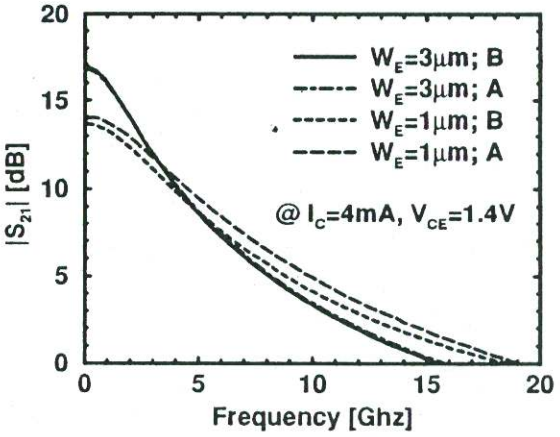

Figure 8: Magnitude of S_{21} scattering parameter.

demonstrates that the surface recombination mechanisms are very important for these devices. Fig. 10 shows that one hour of electrical stress performed on a type A transistor gives rise to an increase of the DC current gain. Similar results were obtained by stressing type B devices, even if, in this case, the exhibited variations are larger.

Fig. 11 reports the effect of the stress on the input noise voltage: a large reduction of the lorentzian component for both types of transistors has been observed. Even for the noise, the type B exhibits a larger variation. It is worth noticing that the larger the DC gain variations, the larger the input voltage noise variations. It is suggested that the increase of the DC gain is correlated with the decrease of the lorentzian component of the input voltage noise and therefore with recombination mechanisms. In order to proof this proposition, we have monitored during the stress the base current. The results are shown in Fig. 12: it appears that the stress firstly reduces the base current, this demonstrating the decrease of recombinations. This phenomenon was reported in the literature with the name of *burn-in effect* [10]. Fig. 12 also shows that the larger the stress current density, the larger the base current variation. In addition, we observe that, under the same stress conditions, type B devices exhibited a larger variation. Moreover, for type B devices, at the higher stress condition, an increase of the base current appeared. Although we do not have enough data to justify this phenomenon, we believe that it is related with the worse quality of the surface of the extrinsic base.

4 Conclusions

In the present work we have demonstrated that C-doped HBT's have better DC, RF, LFN performance and a lower sensitivity to the current stress with respect to the In/C-doped HBT's , thanks to a better extrinsic base surface quality. We cannot state that the presence or the absence of Indium in the base layer makes the difference between the two technologies. However, we believe therefore that at least at this level of Carbon concentration, the Indium codoping is not indispensable. Efforts are certainly needed in order to improve the quality of the passivation/semiconductor interface in the extrinsic base surface region.

Moreover, we believe that the burn-in effect is related to surface recombination mechanisms: the better the surface quality, the lower the burn-in effect.

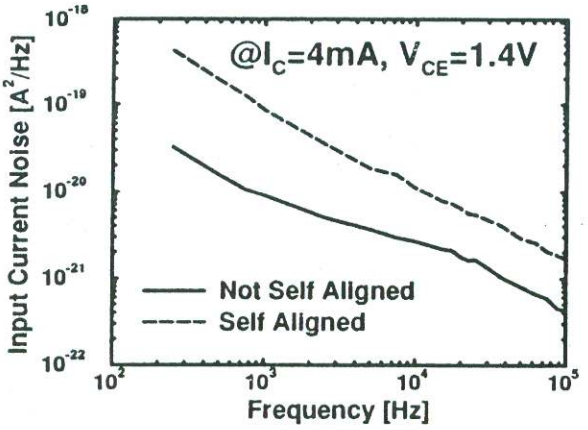

Figure 9: Input Current Noise for HBT's of type B with W_E=3μm.

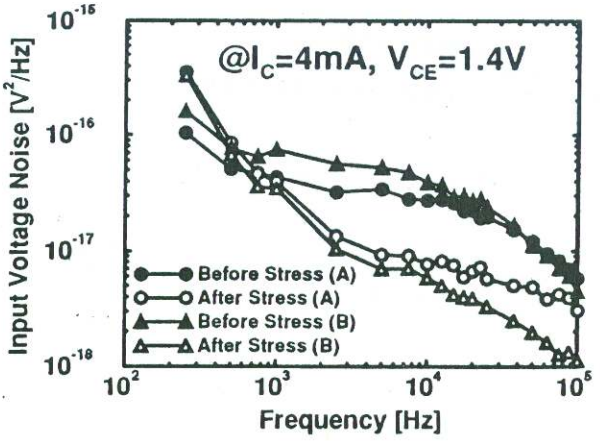

Figure 11: Input Voltage Noise for type A and B HBT's.

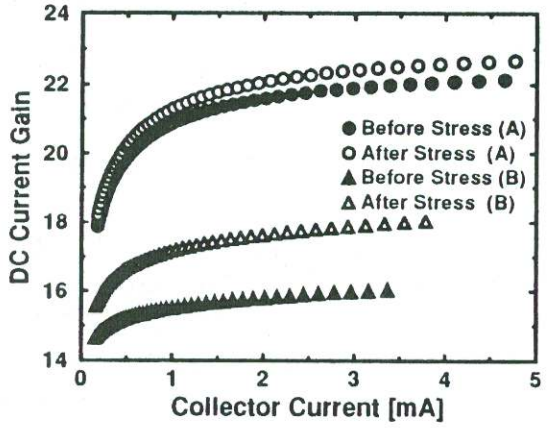

Figure 10: DC current gains for type A and B HBT's.

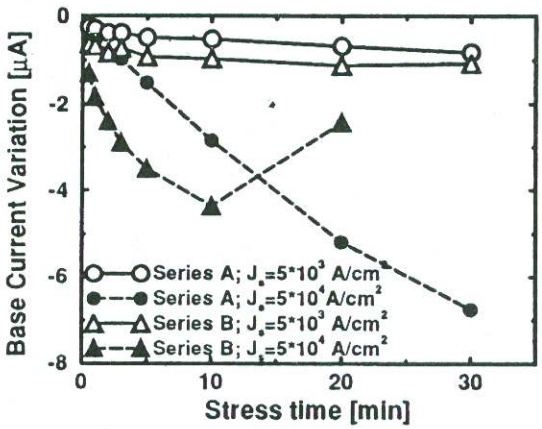

Figure 12: Base current variation vs. stress time.

References

[1] W.J.Ho, M.F.Chang, A.Sailer, P.Zampardi, D.Deain, B.McDermott, R.Pierson, J.A.Higgins, J.Waldrop IEEE *Electron. Device Lett.*, Vol. 14, No. 12, 1993, pp. 572-574.

[2] W.Liu, S-K. Fan, T.Henderson, D.Davito, IEEE *Electron. Device Lett.*, Vol. 14, No. 4, 1993, pp. 176-178.

[3] T.Oka, K.Ouchi, T.Nakamura, *Electronics Letters*, Vol. 33, No. 4, 1997, pp. 339-340.

[4] R.Plana, B.van Haaren, L.Escotte, S.L.Delage, H.Blanck, J.Graffeuil, IEEE *Electron. Device Lett.*, Vol. 18, No. 3, 1997, pp. 108-110.

[5] H.Sugahara, *International Journal of High Speed Electronics and Systems*, Vol. 5, No. 3, 1994, pp. 381-393.

[6] T.Nittono, N.Watanabe, H.Ito, H.Sugahara, K.Nagata, O.Nakajima, Bipolar Transistors", *Jpn. Journ. Appl. Phys.*, Vol. 33, Part 1, No. 11, 1994, pp. 6129-6135.

[7] N.Hayama, K.Honjo, IEEE *Electron. Device Lett.*, Vol. 11, No. 9, 1990, pp. 388-390.

[8] W.Liu, D.Costa, J.Harris, *Appl. Phys. Lett.*, Vol. 59, No. 6, 1991, pp. 691-693.

[9] S.Tiwari, D.J.Frank, IEEE *Trans. on Electron. Devices*, Vol. 36, No. 10, 1989, pp. 2105-2121.

[10] T.Henderson, V.Ley, T.Kim, T.Moise, D.Hill, *Proc. IEDM*, 1996, pp. 203-206.