# Availability of Enabling Technologies for GaAs-Based Specific Applications

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***Abstract*** **- The key technological parameters for processing devices and IC's based on epitaxial structures and semi-insulating GaAs are described. Technological potentialities for various specific applications (analog, digital, radiation detection) are demonstrated. Possible "niches" of technology implementation are discussed.**

## I. Introduction

To achieve success in the field of research and applications under conditions of severe competition on the market of GaAs technology it is very important to find one's own "niche".

One of these possibilities is a low-priced but nevertheless professional and reliable service with a variety of GaAs semiconductor products not readily available from the shelf, especially in small quantities, but tailored to customers' specific application niches. In this context it is important to have a complete set of facilities and well-mastered enabling technologies for several applications [1-3].

In the work key technological processes and their parameters are described for different starting materials and device applications (analog and digital IC's, radiation detectors).The results of modeling and measurements are given. The possibilities of technology implementation are assessed.

## II. Materials and Facilities

Epitaxial structures distinguished by growth method, layer architecture and parameters, as well as by cost were investigated for analog and digital applications (MESFET , δ-FET and HEMT). Taking into consideration that MBE MESFET *a priori* should have better parameters than MOVPE MESFET, whereas the latter are much cheaper, it was interesting to get information on limiting potentialities of these structures with identical parameters and processes in the same technological cycle. Similarly, it was also interesting to compare the characteristics of MBE grown δ-FET and HEMT. And finally, to create radiation detectors semi-insulating (SI) GaAs substrates and MOVPE PIN structures were used as a starting material.

A CAD-room with local network equipped with up-to-date hardware and software (HP ADS, Version 2003) was intended to model, simulate and design layouts. The instrumentation for device characterization up to 26 GHz is also available. A well-equipped pilot line with clean rooms includes process-controlled DUV contact lithography systems, machines for metal (electron-beam and thermal) and dielectrics (pyrolythic, thermal, electron-beam and plasmachemical) deposition, equipment for dry and wet etching, ion implantation, rapid annealing as well as wafer thinning, scribing and packaging. Optical and electric methods are used to control the technology quality.

All layouts include chips with test elements allowing assessment of parameters of ohmic contacts and Schottky barriers, two-level metallization, intercomponent insulation regions. To fabricate radiation detectors special test chips allowing control of bulk material properties in addition to technological parameters were developed.

## III. Technological Processes

In Table 1 key technological characteristics for different process applications are given.

Fine-line patterning of our process goes down to a critical dimension of 0,6 μm. Metallic layers are formed by the lift-off method.

Optimizing investigations were carried out to obtain intercomponent insulation regions formed by ion implantation followed by annealing. After theoretical calculations of the $B^+$ and $F^+$ ion distribution profile for different acceleration energies fluorine was selected as an implanted impurity which appeared to be sufficiently universal. Implantation and rapid annealing (compatible with the ohmic contact formation regime) processes could be selected for this impurity. They give low leakage currents, stable and reproducible results for different epitaxial structures (Fig.1) An important feature for the developed technology is a possibility to replace mesa-

| Item | Material | Parameters | | |
|---|---|---|---|---|
| Ohmic contacts<br>• MESFET<br>• Heterostructure FET<br>• PIN structures | <br>Au/Ge/Ni/Au<br><br>Zn/Au (for p-type) | Resistance, Ohm·mm<br>0,12-0,15<br>0,4-0,7<br>0,12-0,15 | | |
| Schottky contacts<br>• MESFET<br>• Heterostructure FET<br>• SI GaAs | Ti/Pt/Au | Barrier height, eV<br>0,76<br>0,82-0,84<br>0,82-0,85 | Ideality factor<br>1,094-1,23<br>1,088-1,097<br>1,25-1,30 | |
| Two-level metallization | Ti/Pt/Au<br>Ti/Au | Surface resistance, Ohm/□<br>up to 0,08-0,09 | | |
| Intercomponent insulation<br>• MESFET<br>• Heterostructure FET | $F^+$ ion Implanted | Leakage current, μA/mm<br>(at $E=1\cdot10^4$V/cm)<br>about 1,2<br>about 0,3 | | |
| Thin-film resistors | NiCr (80:20)/Pt | Reduced resistance, Ohm/□<br>50±2 | | |
| Dielectrical coatings for: | | Thickness, μm | Breakdown field,V/cm | ε |
| • interlayer insulation | $SiO_x$ (pyrolithic)<br>Polyimide | 0,30-<br>0,32 | <br>No less | 5,5<br>4,7 |
| • MIM capacitors | $SiO_x$ (electron-beam)<br>$Si_3N_4$ (plasmachemical) | 0,13-0.15<br>0,11-0.12 | than<br>$1\cdot10^6$ | 7,0<br>6,8 |
| • pixel matrix passivation (to be selected after flip-chip processes) | $SiO_x$ (thermal)<br>$Si_3N_4$ (plasmachemical)<br>Polyimide | ≥0,5 | | 6,8<br><br>4,3 |

TABLE 1
CHARACTERISTICS OF TECHNOLOGICAL PROCESSES

etching still widely used for "thin" heterostructures by ion implantation[3].

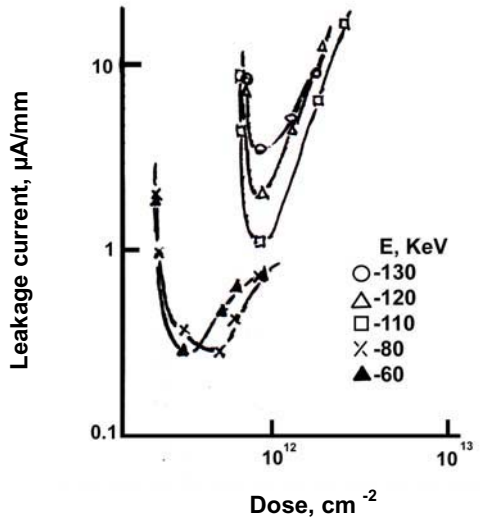


Fig. 1. Leakage currents vs dose for several energies of $F^+$ implantation into MESFET (1-3) and heterostructure FET (4-5)

The methods of deposition of dielectric coatings were developed and optimized depending on their application (see Table 1).

The process flows involved both wet and dry etching or their combination. Transistor channels and via-holes in GaAs were etched by the wet technique while dielectric films ($SiO_x$ and $Si_3N_4$) were etched by the RIE method.

Fig.2 shows windows in $SiO_x$ for a 256x256 pixel matrix (see also Table 1).

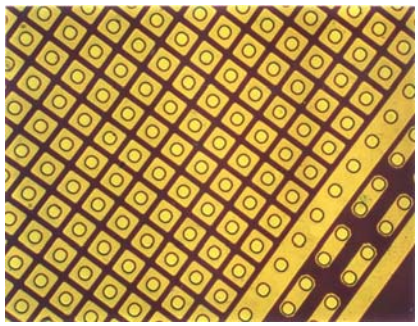

Fig. 2. Section of 256x256 pixel matrix with 55 μm pitch and $SiO_x$ passivation (layer thickness 0,5 μm)

The final stage of processing active and passive elements is the formation of via-holes on the backside of the wafer thinned to 120μ.

All the technological processes are well characterized.

## IV. TECHNOLOGY IMPLEMENTATION

Based on the elaborated technological processes and flows, active and passive components of analog and digital IC's were fabricated and characterized (Table 2). The components for analog applications are compatible with the MMIC technology.

Cutoff frequencies of FET's and RF characteristics of passive components were established according to the results of S-parameter investigations on via-hole wafers.

Table 3 shows the technology potentialities according to simulation results of IC's based on the elaborated library components.

| Active components | Transistor parameters at the gate length 0,8μm and the gate width 100μm | | | | Gate parameters of digital IC's | | |
|---|---|---|---|---|---|---|---|
| | Max.extrinsic transcon-ductance, mS/mm | Output conductivity, mS/mm | Voltage range of transfer characteristics linearity, $V/V_p$ | Cutoff frequ ency, GHz | Delay time, ps | Dissipation power, mW less than | Gate type |
| MOVPE MESFET | 150-160 | 0,70-0,80 | 0,20 | 10-11 | 80-85 | 15 | BFL |
| MBE MESFET | 170-190 | 0,30-0,40 | 0,43 | 12-14 | 65-75 | 12 | BFL |
| MBE δ-FET | 220-260 | 0,21-0,22 | 0,60 | 18-20 | | | |
| MBE HEMT | 290-310 | 0,18-0,20 | 0,65 | 23-25 | 40-45 | 1,3 | DCFL |
| Passive components | Low-frequency parameters | | | Frequency range up to, GHz | | | |
| Thin film resistors | Reduced resistance 50±2 Ohm/□ | | | 13 | | | |
| MIM capacitors | Reduced capacitance 0.60±0.06fF/μm$^2$ | | | 14 | | | |
| Spiral inductors | Inductance range 3-10nH | | | 13 | | | |

TABLE 2
EXPERIMENTAL CHARACTERISTICS OF IC COMPONENTS

| Analog Applications | | Digital Applications | |
|---|---|---|---|
| Type of Devices | Specifications | Type of Devices | Specifications |
| Power Amplifier on MOVPE MESFET | RF frequency-6 GHz, Gain-25 dB, Output Power-20 dBm | Frequency Divider 2/4/8/16 on MOVPE MESFET | Max. input frequency: 7 GHz, Power dissipation: 15mW/Gate (BFL ) |
| Mixer on MBE MESFET | RF frequency-10 GHz, IF frequency-DC-1000 MHz, LO-IF isolation -25 dB | Multiplexer 1:4 on MBE MESFET | Maximum operating frequency: 8 MHz Power dissipation: 15mW/Gate (BFL ) |
| Low Noise Amplifier on MBE δ-FET | RF Frequency-12 GHz, Noise Figure-0.8 dB, Output Power Gain-10 Bm | Demultiplexer 4:1 on MBE δ-FET | Maximum operating frequency: 12 MHz Power dissipation: 15mW/Gate (BFL ) |
| Microwave Sensor on MBE HEMT | RF frequency-12 GHz, Output power gain-10 dBm | Frequency Divider 2/4/8/16 on MBE HEMT | Max. input frequency: 12 GHz, Power dissipation: 1.5mW/Gate (DCFL ) |

TABLE 3
SIMULATED CHARACTERISTICS OF IC'S

The data of experimental and theoretical investigations enable one to optimize the selection of epitaxial structures for particular applications taking into account that MOVPE MESFET's, although a bit inferior in parameters, are less expensive as compared to MBE MESFET's, and that δ-FET's yield rather similar parameters but have a simpler structure as compared to HEMT's [2].

And finally, the developed technology allows to create pixel matrices of higher complexity for radiation detectors.

## V. CONCLUSIONS

Our R&D work resulted in the availability of the enabling technology to process MMIC's for frequencies up to 12 GHz and digital IC's of medium-scale integration based on GaAs and related compounds. The relation between device parameters and type of starting material is established, which allows one to satisfy device requirements with allowance for the cost of epitaxial structures. It is shown that the developed technology can also be successfully used to fabricate pixel matrices based on SI GaAs and PIN-structures for radiation detectors.


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