An Array-Based Design Methodology for 10 GHz SiGe LC Oscillators

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Abstract — **In this paper, a mask programmable array-based design methodology is used for the first time to implement a 10 GHz LC oscillator in a SiGe bipolar technology. The array used was not optimised prior to this design for the development of such circuits, and is used to highlight some of the restrictions faced by the designer when adopting an array-based approach. 10 GHz operation is demonstrated with a phase noise of –85.5 dBc/Hz @ 1MHz on first pass silicon. Whilst this performance is inferior to a full custom LC solution, the array-based design exceeds significantly the performance levels obtainable from a ring oscillator implemented using full custom techniques which meets the SONET jitter specifications. Detailed analysis of the various phase noise contributions to the 10 GHz LC oscillator show that the performance is not prohibitively compromised by the array-based design approach. Together with the improved time-to-market resulting from an array-based approach, this work makes a compelling case for the viability and adoption of array-based design methodologies for a wide range of RF and microwave applications.**

I. Introduction

The consumer electronics industry is becoming steadily larger as more and more people get involved in multimedia and communications. This increase in the size of the market has resulted in a marked increase in the number of companies offering products and services in the communications sector, bringing with it increased levels of competition. As this competition increases, the choice for the consumer becomes greater but more work has to be done by a company in order to secure sales and revenue, growth, and ultimately survival. While improved product quality and functionality is a key differentiating factor between competitors, this is increasingly giving way to improved time-to-market as one of the main contributors to market growth. In order to improve product time-to-market a host of new design techniques and methodologies are emerging for integrated circuit design, which maintain expected performance levels while decreasing the design and manufacturing cycle times associated with product development. One such methodology is that of array-based design. This particular methodology, while being hugely successful in the digital field has not seen similar breakthroughs in the RF and microwave arena due to perceptions of design and performance limitations that result from such an approach. This research takes a 10 GHz LC oscillator, a high performance RF circuit, and implements it using a mask programmable array-based design methodology as a test vehicle to explore the performance limitations arising from adopting an array-based approach. The aim of this work is to establish whether an array-based LC oscillator is capable of outperforming a custom ring oscillator solution which meets the SONET specification for 10 Gbit telecoms requirements. The target for success in the array-based LC oscillator was therefore oscillation at 10 GHz with a phase noise better than –78 dBc/Hz at 1 MHz offset [1].

II. The Target Array

To investigate the proposal that a high quality LC oscillator can be implemented using an array-based design approach, a suitable platform must be selected on which to develop it. In this work, an existing full custom chip for another 10 GHz application was chosen. The motivation for this approach is that prior to the definition of the upper metal layers, any full custom design can be considered as a "sea of unconnected components" which can be wired up to implement a new design. Although the components are placed in ideal locations for the full custom design, they bear little or no relation to the new design. In reality, it is likely that the performance of the array-based design will be impaired rather than assisted by the location of the components. Adopting this approach is therefore a very stringent test of the viability of an array-based methodology. Figure 1 is a layout of the full custom "target array" 10 GHz component, realised using a 0.6 μm SiGe bipolar technology with an f_T of 45 GHz.

The greatest problem with the selection of this particular array is that it contains no inductor and therefore has no dedicated area available for the spiral required in the LC oscillator. This was one of the most critical design issues in the investigation of the oscillator circuit and the selection of the target array. In order to allow the design process to continue it was necessary to find a location on the die, suitable for the placement of the spiral.

Three criteria were used to select the optimal spiral location:

i. keep the spiral as close to the tank capacitors as possible to minimise tank losses
ii. keep the tank circuit as close to the main oscillator circuit as possible

iii. ensure that the spiral is not placed on top of any other circuitry

Based on maintaining these rules, Figure 2 shows the location of the main building blocks of the 10 GHz LC oscillator including the location chosen for the spiral.

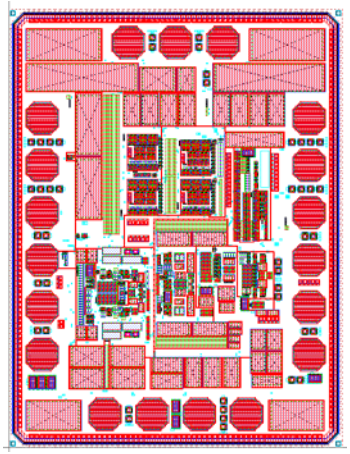

Fig. 1. The target array.

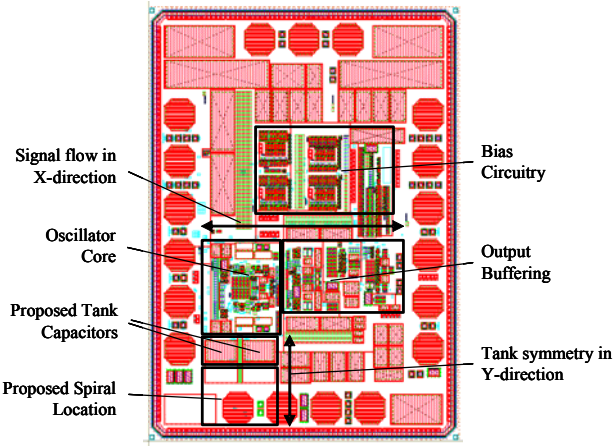

Fig. 2. Mapping of the LC oscillator blocks onto the target array.

III. Circuit Design

A. Inductor Design

A centre-tapped inductor was used in the LC tank circuit to reduce the area of the inductor, thereby easing its placement into the target array. In addition, a centre-tapped inductor has a higher Q factor and its inherent symmetry is important for differential design [2]. The spiral was designed to minimise series resistance and substrate losses. Figure 3 shows the equivalent circuit of the centre-tapped spiral inductor, from which a number of loss mechanisms associated with the implementation of a planar inductor on a silicon substrate can be deduced.

As well as the series resistance of the spiral, capacitive coupling allows interaction with the substrate where image currents can flow. The flow of these image currents is in opposition to the normal spiral current introducing extra losses not seen in discrete components.

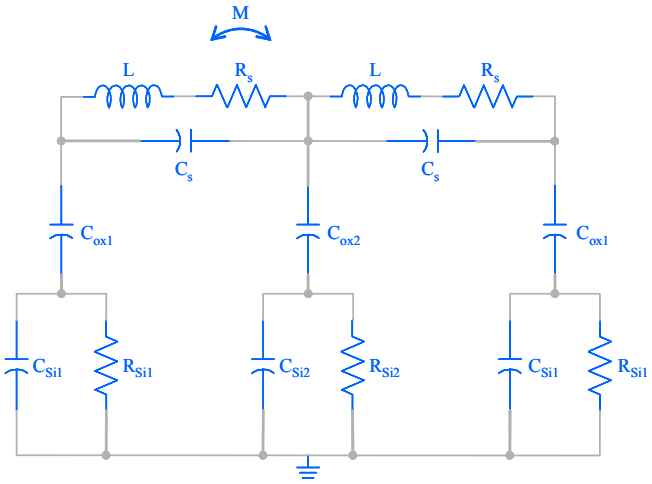

Fig. 3. Losses associated with the monolithic implementation of planar spirals

A 0.5 nH spiral was designed for 10 GHz operation of the spiral. The dimensions of the spiral are shown in Table I.

Description	Value
Inductance	0.5 nH
DC series resistance	1.3 Ω
Radius	63 μm
Track width	14 μm
Track spacing	2 μm
Number of turns	2

TABLE I
SPIRAL DESIGN DIMENSIONS

The associated model parameters for the spiral are shown in Table II.

Model Component	Description	Value
L	Spiral inductance	0.19 nH
M	Mutual inductance	0.06 nH
R_s	DC series resistance	0.65 Ω
C_s	Feedthrough capacitance	2 fF
C_{ox1}	Oxide capacitance	20 fF
C_{ox2}	Oxide capacitance	40 fF
R_{Si1}	Substrate resistance	800 Ω
R_{Si2}	Substrate resistance	400 Ω
C_{Si1}	Substrate capacitance	0.26 fF
C_{Si2}	Substrate capacitance	0.52 fF

TABLE II
SPIRAL MODEL PARAMETERS

These model parameters were used in the simulation of the overall oscillator circuit.

B. Oscillator Design

The schematic of the LC oscillator design is shown in Figure 4. The circuit architecture is based on a cross-coupled pair for the oscillator core, with the addition of a capacitive feedback loop to increase the output signal amplitude and minimise phase noise, $L(\Delta\omega)$, as dictated by Equation 1 [3].

$$L(\Delta\omega) = 10\log\left[\frac{2kT}{P_{sig}}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \quad (1)$$

where k is Boltzmann's constant, T is temperature, ω_0 is the oscillation frequency, P_{sig} is the signal power, Q is the quality factor of the tank and $\Delta\omega$ is the offset frequency at which the noise is measured

A number of output buffer circuits were included to enable on-wafer characterisation in an environment, leading to the requirement for DC level shifting to ensure optimal circuit performance.

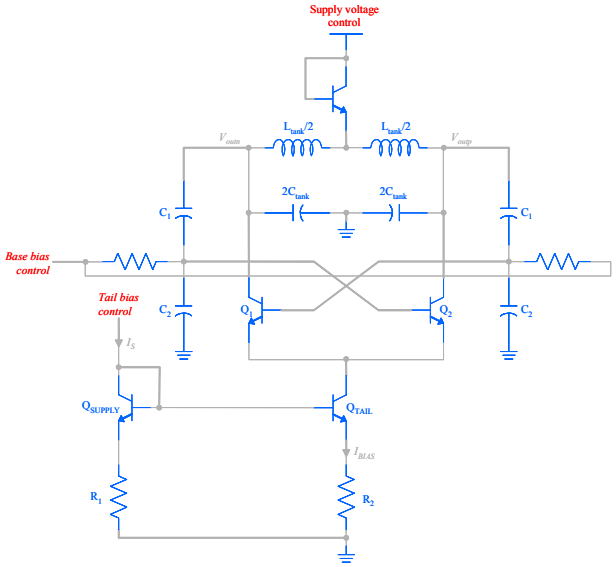

Fig. 4. LC oscillator schematic showing control voltages.

Finally, to improve testability, a range of reference circuits and external bias control terminals were included to control the tail current, cross-coupled device bias voltage, output buffer bias voltage and supply voltages. Following layout, back annotation enabled the impact of parasitics to be assessed and mitigated by final redesign, in particular adjustment of capacitance values in the tank circuit.

IV. Oscillator Performance

The implementation of the circuit on silicon is shown in Figure 5. First pass silicon was evaluated and oscillation in the range 10.14 GHz to 10.22 GHz with output power in the range –16 dBm to -12 dBm, dependent on applied bias as shown in Figures 6a and 6b, was observed.

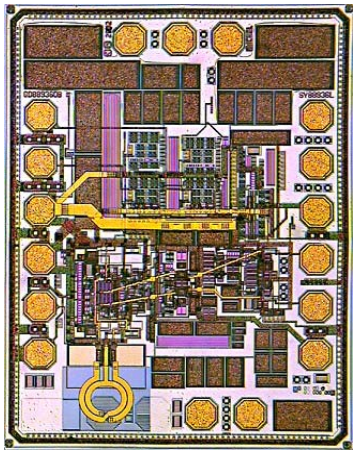

Fig. 5. Die photograph of completed LC oscillator.

Figure 6c shows the phase noise at an offset of 1 MHZ as a function of applied bias. Under designed conditions, the whole circuit draws a current of 38 mA, with a centre frequency of 10.17 GHz and a phase noise of –85.5 dBc/Hz @ 1 MHz offset – in line with circuit simulation and meeting the phase noise target outlined above.

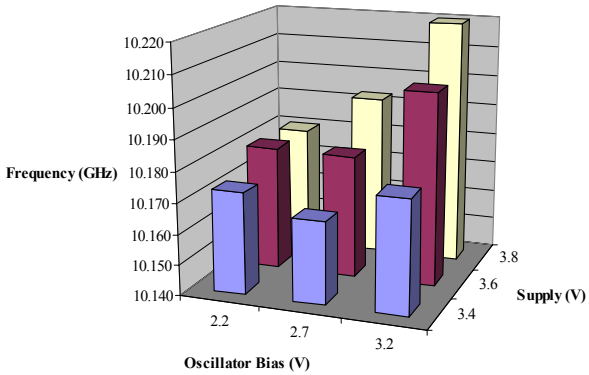

Fig. 6a. Relationship between the centre frequency of the oscillator and the applied bias voltages.

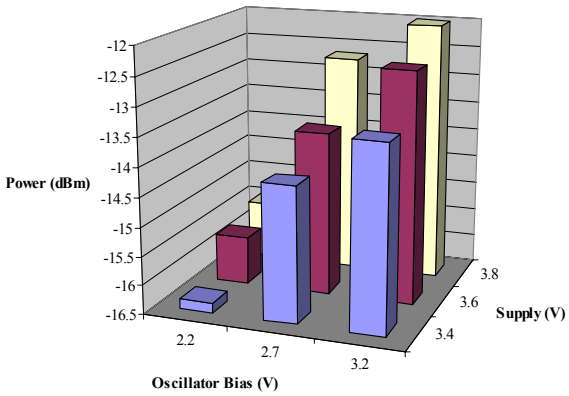

Fig. 6b. Relationship between the output power of the oscillator and the applied bias voltages.

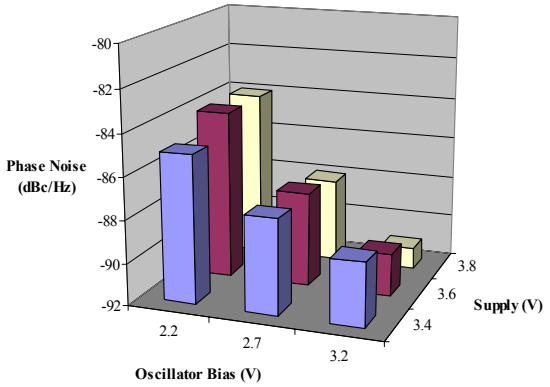

Fig. 6c Relationship between the phase noise performance of the oscillator and the applied bias voltages

To understand where the various phase noise contributions arise in the circuit, detailed investigations such as a study of the tank circuit losses including the influence of the skin-effect in the series resistance of the inductor, together with an impulse sensitivity function at key circuit nodes [4] have been undertaken. Table III summarises the conclusions of the phase noise study, whilst Figure 7 shows the agreement obtained between measurement and calculation of phase noise.

Noise Source	Phase Noise (Noise/Signal)	Phase Noise (dBc/Hz)	% Contribution
Supply voltage noise	1.226×10^{-9}	-89.12	52 %
Collector current shot noise	$2 \times 3.047 \times 10^{-10}$	-92.15	26 %
Base resistance noise	$2 \times 2.262 \times 10^{-10}$	-93.44	19 %
Tank losses, thermal noise	$2 \times 2.976 \times 10^{-11}$	-102.3	2 %
Bias current noise	2.112×10^{-11}	-106.75	1 %
Total oscillator noise	2.368×10^{-9}	-86.26	100%

TABLE III
INDIVIDUAL CIRCUIT CONTRIBUTIONS TO PHASE NOISE

This analysis shows that the major contributors to the phase noise performance are unrelated to adopting array-based design methodology. The supply voltage phase noise arising from a lack of suitable decoupling capacitors on the target array can be easily overcome in future target arrays, whilst the collector current and base

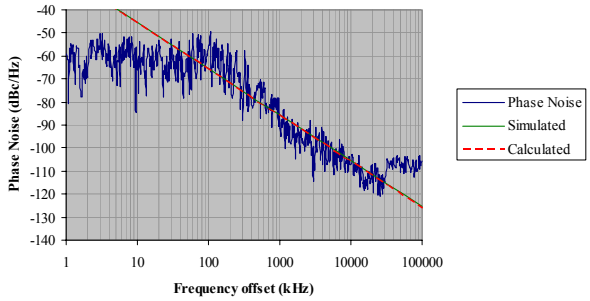

Fig. 7. Comparison of measured, simulated and calculated phase noise

resistor phase noise contributions are technology limited rather than layout constrained.

VI. CONCLUSION

This work demonstrates that a high performance 10 GHz LC oscillator can be realised using an array based design methodology. The aim of the work was not to demonstrate the ultimate phase noise performance, rather that an array-based approach can deliver sufficient phase noise performance to surpass that of a full custom ring oscillator solution which meets the SONET jitter specification. The achievement of this target, together with the improved time-to-market resulting from an array-based approach, make a compelling case for the viability and adoption of array-based design methodologies for a wide range of RF and microwave applications.

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