Power Performance Evaluation of AlGaN/GaN HEMTs through Load Pull and Pulsed I-V Measurements

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Abstract — **A systematic evaluation of power performances of AlGaN/GaN HEMTs has been performed by means of CW on wafer Load Pull measurements at X band. Those measurements have been correlated to the results obtained through I-V and S-parameters pulsed measurements and a strong correlation has been found between the two types of measurement. Power up to 6Watts has been measured on a 1.2 mm device that can be further improved if trapping effects can be removed. A non linear electrical model of the 0.25x 1200 µm² transistor taken from the I-V and the S-parameters pulsed measurements is validated by CW load pull measures.**

I. INTRODUCTION

The development of Field Effect Transistors on wide bandgap materials has raised a strong interest for solid state power generation at microwave frequencies [1], [2]. Indeed the high breakdown voltages induced by the wide bandgap as well as a very high thermal conductivity for SiC and a medium one for GaN allow very high drain biasing conditions. In the case of AlGaN/GaN HEMTs very high electron sheet densities, up to 1.5 10^{13} cm^{-2}, can be obtained leading to high drain current densities, up to 1.4A/mm for 0.25 µm gate length devices. Those characteristics lead to a significant potential increase of the power density that can be achieved.

Record power densities of 9.4W/mm at 8GHz [3] have been obtained under pulsed measurement conditions with conventional gate GaN-based HEMTs, whereas they reach 30.6W/mm at the same frequency with optimized field plates [4].

However when operated under CW conditions, the power achieved is strongly reduced due to self heating effects on one hand and trapping effects on the other hand [5], [6]. Thus it is relevant to correlate the microwave power performances of AlGaN/GaN HEMTs measured on wafer at 10GHz to the measurements obtained from pulsed I-V, pulsed S-parameters measurements.

This comparison allows an in depth evaluation of the effects of traps thanks to the output characteristics and it is shown that a rough estimation of the output power available can be given using the pulsed I-V characteristics. Moreover it is also shown that removing trapping effects could lead to a significant increase of the output power. All those results have been confirmed by a set of measurements on 1mm and 1.2mm devices from different manufacturers.

II. MEASUREMENT SET-UP

In order to evaluate the correlation between output power and pulsed I-V characteristics, the two kinds of measurements have been performed on wafer on 1mm and 1.2 mm total gate periphery devices. Pulsed I-V and pulsed S-parameters are measured following the methodology described in [5]. This sequence of quiescent bias permits to determine the location of the traps and the load line limitation due to this phenomenon at microwave frequencies. Those hypothesis have to be confirmed through high power load pull measurements. Thus CW load pull measurements on wafer have been performed. The load pull set up used is described at *Figure-1*.

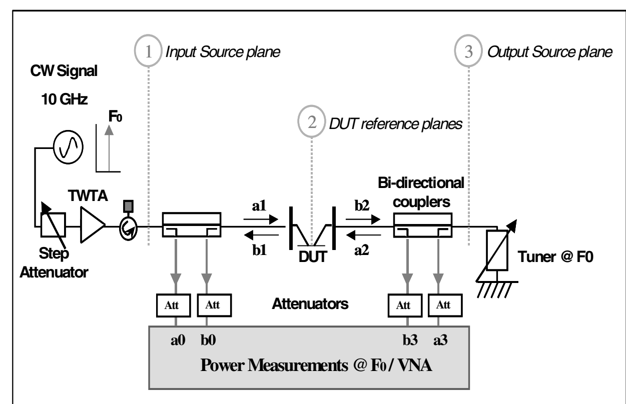

Fig-1: *Synoptic presentation of the load pull measuring bench*

This setup is mainly composed of a power amplifier associated with a controlled step attenuator to route the signal with a controlled RF power level toward the DUT. The transistor is matched at the fundamental frequency (10GHz) in order to optimize the output power. The output terminations at harmonic frequencies are set to 50Ω. Source terminations are also set to 50Ω. By the use of a VNA, AM/AM and AM/PM measurements are performed. For this purpose, a classic calibration (LRM)

is firstly performed at the DUT reference planes. Then, using a power meter, an absolute power calibration is made at both input and output source planes. In order to obtain an error corrected value of this power at the DUT reference planes for on-wafer probe contacts, reciprocity relationships are used [7].

III. MEASUREMENT RESULTS

Measurements have been performed on various transistors fabricated by different manufacturers on SiC substrates coming from various suppliers. They confirm the results presented in this paper on a 0.25x1200 µm² transistor which is made of 12x100µm width fingers. The transistors were processed on a 330µm SiC substrate from QINETIQ by the TIGER labs. At first a complete characterization of the transistors has been performed for three quiescent bias points Vdso, Vgso [5]. The bias point corresponding to Vdso=0V and Vgso=0V serves as a reference for the subsequent measurements. Indeed the current obtained in this configuration is maximum as the trapping effects are minimized. The transistors have been measured for gate voltages up to 2Volts. The results shown at *Figure-2* demonstrate a maximum current density of 1.4A/mm when the transistor is biased at Vgso=0V and Vdso=0V (the blue curves). This maximum current is reduced to 1A/mm when a quiescent gate bias of -8V is applied to the gate (the black curves).

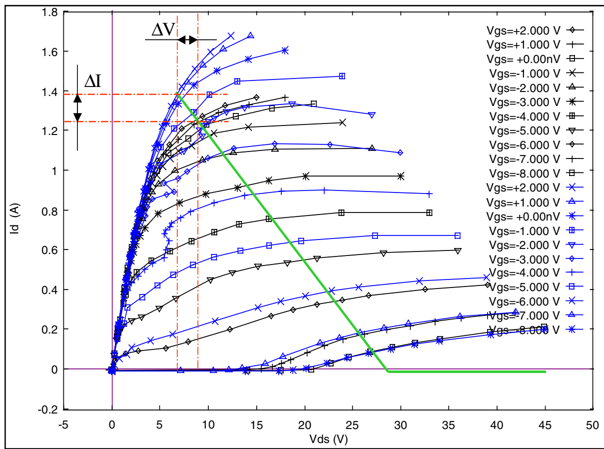

Fig-2: *Comparison of Output characteristics measured at two different quiescent gate bias*

The traps located at the surface of the transistors are responsible for this decrease of the maximum current. Following the output load line, this decrease of the maximum current corresponds to an increase of the knee voltage thus reducing again the output power. It has to be noticed that the measurements performed for a quiescent drain bias voltage of 25Volts do not exhibit significative differences with the current measured at 0 drain bias, thus demonstrating that traps excited by the longitudinal electric field have a weak effect. Moreover breakdown voltages as high as 90Volts have been measured for these transistors.

The values of the maximum oscillating frequency and of the transition frequency are respectively of 33GHz and 31GHz for an instantaneous bias point (Vgsi=-6V, Vdsi=27V).

Load pull measurements have been performed at 10GHz in CW conditions. The transistor was biased in class AB for Vgso=-6.7Volts and Vdso=25Volts and the load impedance was tuned for maximum output power (Z_L=15 + j 7.3). The bias current was measured at 250mA. However this bias current does not correspond to the measured one in pulsed I-V conditions. This is due to the fact that a low frequency oscillation (~6.7MHz) was observed at low levels of the input signals. This oscillation disappears for input levels higher than 10dBm.

The power transfer characteristics are shown at *Figure-3*, i.e. the gain (*3_a*), the output power (*3_b*) and the power added efficiency (*3_c*). It has to be noted that an output power of 6.7Watts (= 38.2 dBm) has been obtained with a PAE of 40% and an associated gain of 6dB. The small signal gain was estimated at 12dB while it cannot be measured directly because of the oscillation. A rough estimation of the output power is obtained by inspecting the shape of the pulsed I-V characteristics and demonstrates that the main limitation of such devices is related to the trapping effects. Thus reducing those effects will allow to reach the theoretical Johnson limit for output power.

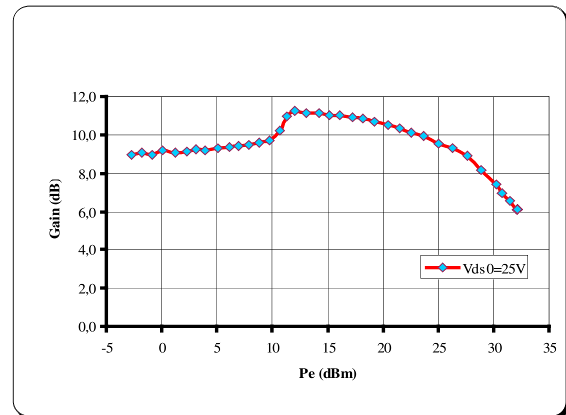

Fig-3_a: *Power gain in dB versus input power in dBm measured @ 10GHz*

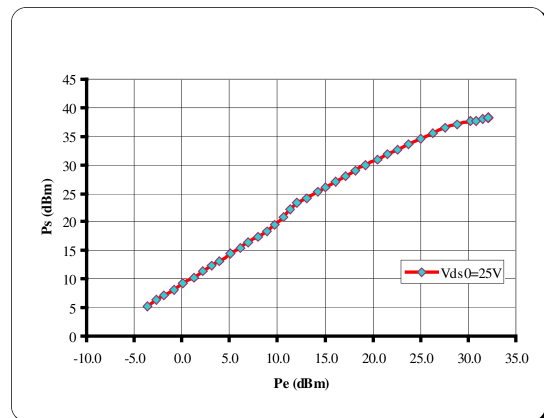

Fig-3_b: *Output power in dBm versus input power in dBm measured @ 10GHz*

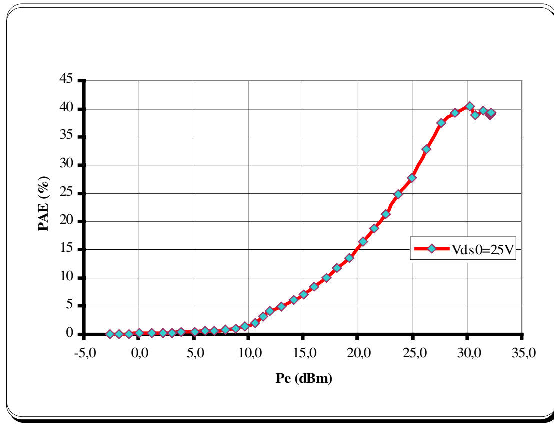

Fig-3_c: *Power added efficiency versus input power in dBm measured @ 10GHz*

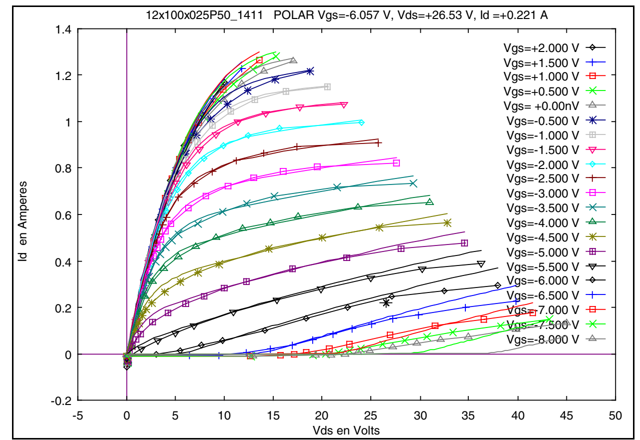

Fig-4: *Comparison between the I-V measurements and model for a quiescent bias point Vgso= -6V et Vdso=26.5V*

V. COMPARISON BETWEEN MEASUREMENTS AND NON LINEAR MODEL

A. Extraction of the non linear model

The 0.25x1200 µm² transistor presented in this paper was modeled thanks to the software developed in the laboratory (IRCOM). The I-V characteristics of this transistor have been measured for a quiescent bias point Vgso=-6V and Vdso=26.5V so as to take into account the parasitic trapping effects which lead to a significant decrease of the output current Id.

The extrinsic and intrinsic transistor parameters of the linear model (*Table-1*) were extracted for the instantaneous bias point Vgsi=-6V and Vdsi=27V closest to the quiescent bias point (Vgso=-6V and Vdso=26.5V) thanks to S-parameters pulsed measurements on the 2-40GHz band.

Rg (Ω)	Lg (pH)	Cpg (fF)	Rd (Ω)	Ld (pH)	Cpd (fF)	Rs (Ω)	Ls (pH)
0.8	75.3	114.9	0.8	77.33	101.6	0.25	14.83
Cgs (fF)	**Cgd (fF)**	**Gm (mS)**	**gd (mS)**	**Cds (fF)**	**Ri (Ω)**	**Tau (ps)**	**Rgd (Ω)**
904.7	130.2	212.5	14.8	319.3	2.51	1.1	20

Table-1: *Extrinsic and intrinsic elements of the 12x100µm model derived at instantaneous bias point (Vgsi=-6V, Vdsi=27V) for a quiescent bias point (Vgs_0=-6V, Vds_0=26.5V).*

Once we know the linear parameters of the transistor, we just have to model the non linear elements : the current source, the drain-gate breakdown generator, the gate-source and gate-drain diodes, and finally the Cgs and Cgd capacitors.

A new algorithm developed within the laboratory and based on the Tajima modified model [8] allows to obtain a model of the current source (*Figure-4*), of the gate-source and gate-drain diodes as well as of the breakdown generator in a precise way.

Eventually, the extraction of the non linear capacitors (Cgs, Cgd) is made along a load line estimated for the bias of a transistor in class AB, in order to have capacitors with one command.

B. Validation of the electrical non linear model in small and large signal.

Finally this non linear electrical model is implanted in a commercial simulator (ADS) so as to compare this model with the S-parameters measurements and the load-pull measurements.

We can notice a good agreement between the S-parameters measurements and model (*Figure-5*) for an instantaneous bias point (Vgsi=-6V, Vdsi=27V).

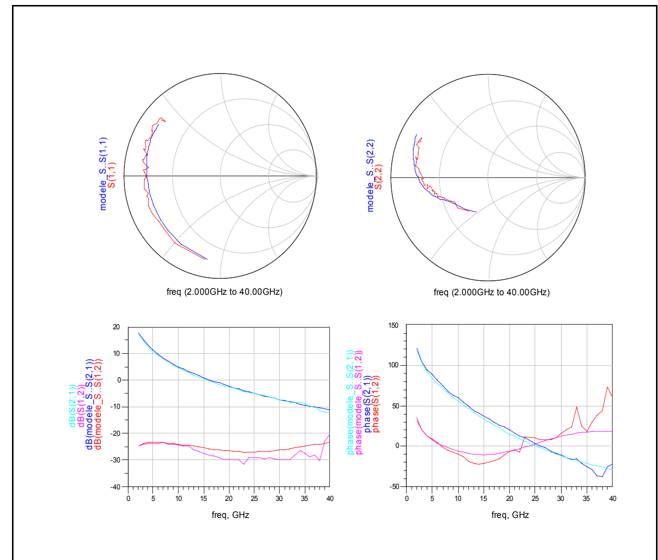

Fig-5: *Comparison between the S-parameters measured and simulated from 2 to 40GHz at an instantaneous bias point Vgsi=-6V, Vdsi=27V*

Figures-6a, 6b, 6c, show the large signal comparisons between the CW load pull simulation and the measurements for a same quiescent bias point (Vdso=25V, Idso=250mA) at the frequency of 10GHz with the same load impedance Z_{load}=(15+j 7.3).

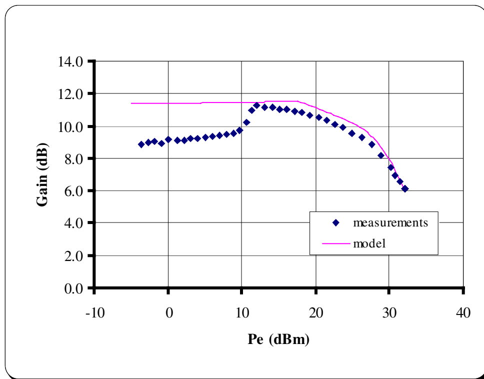

Fig-6_a: *Load-pull results: measured (dots) / simulated (lines) at the power gain (@10 GHz)*

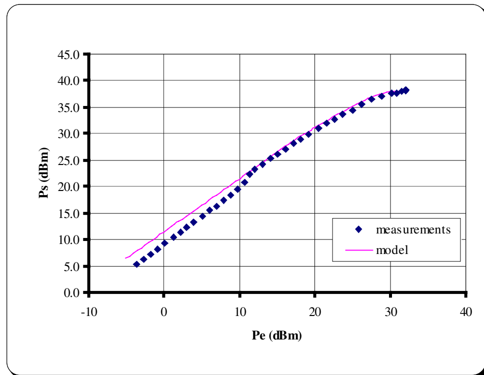

Fig-6_b: *Load-pull results: measured (dots) / simulated (lines) at the output power (@10GHz)*

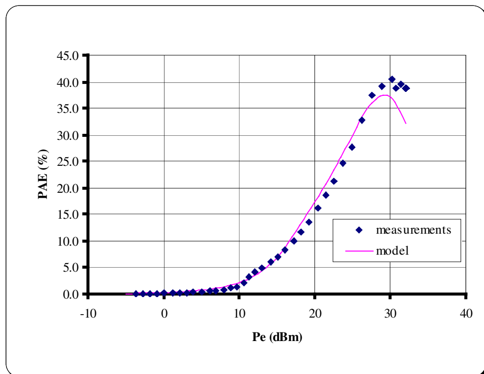

Fig-6_c: *: Load-pull results: measured (dots) / simulated (lines) at the power added efficiency (@10 GHz)*

The good agreement between small and large signal measurements and the simulations of the non linear electrical model allows to validate the model of the 12x100 Tiger transistor. Moreover, it is important to notice that only pulsed measurements enable to highlight the parasitic effects of traps (significant decrease of the output current and consequently decrease of the output power), thus helping to take them into account in the process of modeling the current source. This allows to foresee as accurately as possible the performances of the transistors thus measured.

VI. CONCLUSION

Full characterization of various transistors has been completed demonstrating that the main limitation for output power of AlGaN/GaN transistors is related to surface and buffer traps. The strong correlation obtained from pulsed and load pull measurements confirms this fact. Thanks to the pulsed measurements, we have been able to model precisely the 12x100 Tiger transistor while taking into account the trapping effects. This model thus realized was validated by CW load pull measurements.

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