Millimetre-wave MMIC packaging compatible with surface-mount technology (SMT)

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Abstract —- **This paper presents an interconnect and packaging solution for millimetre-wave MMIC, based on collective wiring and surface mount technologies. The designed structure consists of an SMT CSP (Chip Scale Package) mounted on printed circuit board (PCB). This packaging concept has been applied to a millimetre-wave LNA and has been measured up to 60 GHz, exhibiting results close to bare die measurements (insertion loss per millimetre-wave transition lower than 0.5dB) and demonstrating the potential of this technology up to V-band.**

I. Introduction

Demand from microwave and millimetre-wave module manufacturers is more and more oriented to SMT packaged MMICs, allowing reduction of costs with better interconnect reproducibility, less tuning, compatibility with classical SMT assembly line[1].

Classical SMT packages use wire bonding for MMIC-to-package interconnect. The package is then connected to a printed circuit board (PCB) thanks to via holes and solder [1]. This solution, although advantageous and already under industrialisation, is limited to around 40 GHz.

In order to avoid drawbacks of wire bonding (low reproducibility, parasitic inductance, costly sequential assembly method, additional lid needed…), solutions based on flip-chip MMICs have been proposed [2][3]. These solutions need MMICs in coplanar configuration for good behaviour at high frequencies, and are not easily compatible with mounting on classical PCB, in particular because of small dimensions of interconnect parts on MMIC compared to possible dimensions and tolerances on PCB. An intermediate substrate can be used to compensate for these differences and to make the package compatible with standard SMT assembly (no manipulation of bare dies). Consequently an additional transition is needed between intermediate substrate and PCB.

This paper describes a low cost solution based on a collective wiring technology [4] compatible with microstrip MMICs for low cost packages, directly mountable on standard PCB for applications up to 60 GHz.

The proposed technology uses low loss polymer layers including LCP (Liquid Cristal Polymer) [5]. Interconnects are obtained by etched lines, vias, and solder bumps for surface mounting. The designed CSP (Chip Scale Package) includes the MMIC and the first stage decoupling capacitors.

II. Interconnect & Packaging Structure And Process

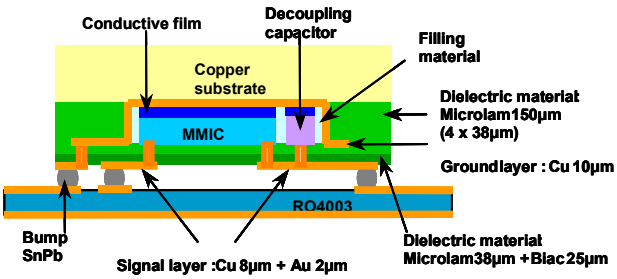


Fig. 1. Interconnect and packaging structure cross-section

Fig.1 is a schematic cross-section of the interconnect and packaging structure mounted on board. The carrier used for package realisation consists of a 450 µm thick copper substrate on which a first dielectric film (prepreg, 150 µm thickness) is laminated. All process operations are done at copper panel level, for several MMICs, before dicing to achieve individual packages. Cavities are laser drilled. MMICs and capacitors are then glued into cavities thanks to a 50 µm thick conductive film. The empty space around dies is filled with epoxy resin to make the surface planar and a second level of polymer is laminated (prepreg + LCP).

Figure 2 shows a millimetre-wave LNA from United Monolithic Semiconductors (UMS) with 100 pF decoupling capacitors (that will be integrated in SMT package) before lamination of the second level of polymer.

To be compatible with the lamination process, the MMICs have to be passivated, which is the case of the used dies provided by UMS (BCB passivation).

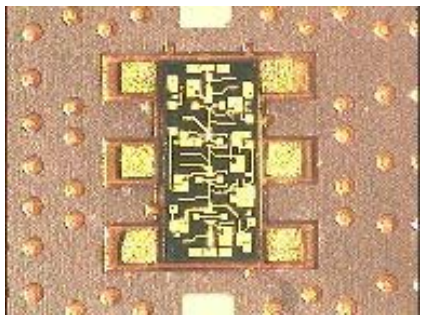


Fig. 2. Millimetre-wave LNA with decoupling capacitors before lamination of second level of polymer

The polymer materials have been chosen taking into account their coefficient of thermal expansion (CTE) to

limit thermo-mechanical constraints. They have also good RF properties (loss tg=0.003 for LCP and 0.008 for prepreg). Via hole drilling is done by laser (as cavities). Metallised areas and lines are obtained by sputtering, electro-plating and photolithography. First electrical tests are performed before bump processing. SnPb bumps are then realised by electrolytic process (bump diameter = 200µm). After dicing, the package is mounted on RO4003 substrate (203 µm thickness) .

III. Electrical Design

Optimisation of millimetre-wave transitions (matching , spurious modes suppression) has been achieved thanks to electromagnetic (EM) simulations performed with HFSS® (Ansoft). Input and output lines on the PCB are shielded microstrip lines. RF lines on the package (and locally on the PCB, close to bump transition) are coplanar-grounded type (CPWG). This allows to limit radiation losses and cross-talk between input and output lines that may cause feedback oscillations. Furthermore, a coplanar mode is needed to achieve a good matching of the "bump transition".
Bumps and via holes are used for grounding and to suppress the propagation of spurious modes between module and board, in the air or in the polymers. This suppression of modes is optimised by removing PCB dielectric material under the MMIC (cavity created in the PCB). Good shielding is then obtained and no additional cap is needed. Figure 3 shows the result of EM design concerning return loss of one transition (one transition = bump + line on polymer + via) and cross-talk level between input and output PCB RF lines.

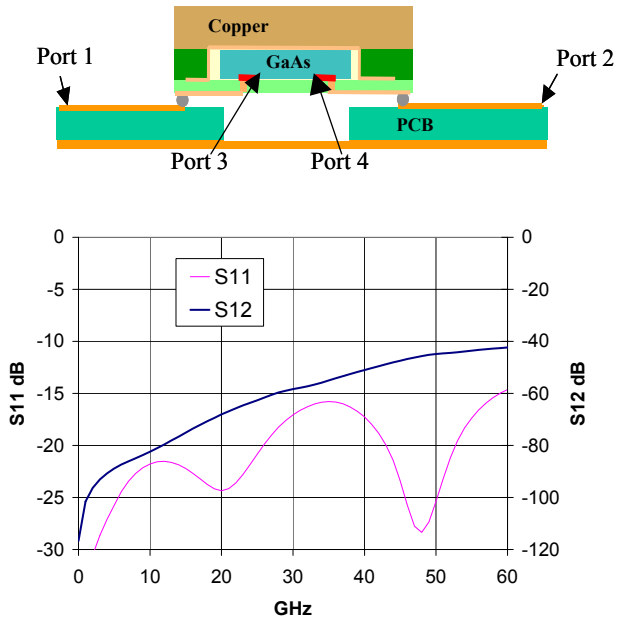


Fig. 3. Simulated structure - Results of EM design : transition return loss, cross-talk coupling.

The simulated response of the packaged die, here millimetre-wave LNA from UMS is obtained with the following steps :

- The passive part of the structure (complete package mounted on board with input and output ports instead of active MMIC) is simulated with HFSS and results are included in a 4 port [S] parameter file (2 ports for input/output and 2 ports for die connection),
- To simulate the response of the packaged die mounted on board, measured S-parameters of the bare die are connected between corresponding access ports of the passive structure simulation.

This is illustrated in figure 4 with the obtained result. The "active" simulation of the complete structure is performed with a circuit software (Serenade®).

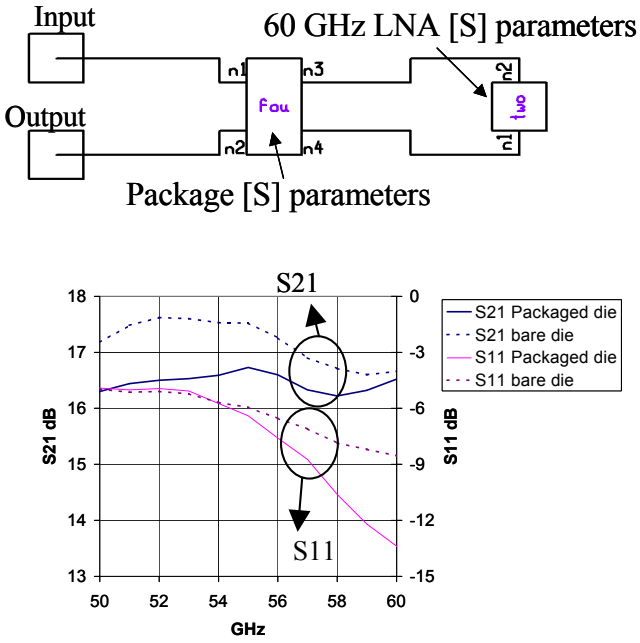
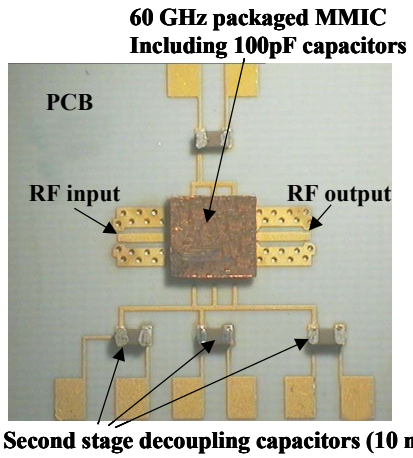


Fig. 4. Packaged die simulation and design result

IV. Test Results

Figure 5 shows the packaged millimetre-wave LNA mounted on board and its associated response compared to typical bare die response. The measured S21 response is presented after correction by removing the losses of shielded microstrip lines on PCB (the presented response includes contributions from MMIC, package and bump transition to the PCB). Typical S21 bare die response has been obtained after measurement of MMICs from the used batch (UMS) ; all MMIC responses from this batch are included in [typical S21] ± 0.5 dB. The size of the package is 3.5*3.8*0.66mm.



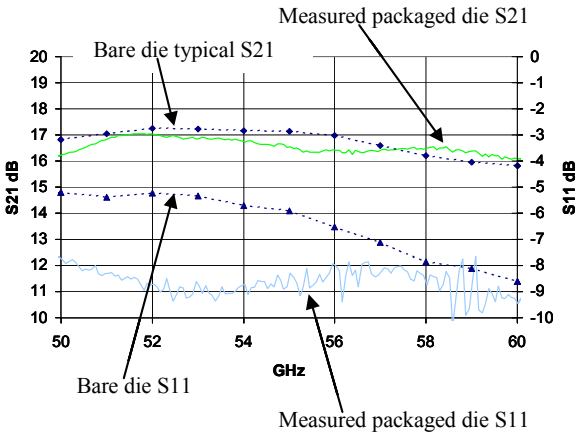


Fig. 5. Photography of packaged MMIC including first stage 100 pF capacitors – Associated measurement

The measured response of the packaged LNA is very similar to the typical response of bare dies.
Insertion losses due to transitions are lower than 1 dB (less than 0.5 dB for input or output transition).
S11 response which is presented is the direct measurement at RF input without correction ; it confirms the matching of the realised structure.
Another important parameter to be controlled is the "cross-talk" level of the packaged die mounted on board, this is the "direct" transmission level between input and output of the die, the power part which is not going through the MMIC but directly from the input to the output of the package, it is of course important to maintain this level as low as possible to avoid any oscillation loop and provoke unstable state of the die.

The packaging of the die and its mounting on board increase this "direct" coupling between input and output of the die, it can be characterized by the parameter S12 of the mounted packaged die compared to the one of the bare die, they should be very similar. The stability of the amplifier strongly depends on this value which should not exceed –40dB typically.

V. Conclusion

The implemented collective wiring technology has demonstrated its capabilities for achieving millimetre-wave SMT CSP working up to 60 GHz. These results are very promising for a future generation of packages, providing a low cost packaging solution with good RF performances and allowing the suppression of wire bond interconnects.

Acknowledgement

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References

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