GaAs, Advanced RF CMOS and Silicon Components for Miniaturised Space Digital Receiver

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Abstract: **This paper presents the electrical and technological design for the new generation of Telemetry and Telecommand (TT&C) receivers for satellite application, in Ka Band. The congestion of the S-band are forcing towards higher frequency bands and towards a bandwidth optimization. The improvements in the system performance, and at the same time reducing cost, mass and power consumption are the goals to achieve with these new developments[1]. Performance repeatability, improved reliability figure, modular design, unit miniaturisation and reduced tuning effort in production are just few of the possible advantages introducing of latest technologies either in the RF/ microwave and in the digital domain.**

I.INTRODUCTION

The TT&C Subsystem allows the two way transfer of information between the satellite and the Ground. The subsystem is composed of an RF Section and of a base-band section; it provides the spacecraft with the capability for receiving up-link command data, transmitting status and data, and transponding ranging signals from and to the ground stations. The new generation TT&C receiver design is based on a digital architecture; this solution represnts allows to meet the functional requirements with the following advantages with respect to the present fully analog solutions:

- Receiver reconfigurability
- Inclusion of data demodulation capability (sub-carrier tracking circuit, bit-synchroniser)
- Data rate flexibility
- Interface optimisation

The Ka-Band Command Receiver frequency plan is based on modern frequency synthesis techniques. On the receiver side the fractional-*N* synthesis approach is used to perform the down-conversion of the received signal from Ka-band down to IF frequency, i.e. 140 MHz, approximately. This architectural solution allows to achieve high frequency resolution (typically of the order of microhertz) and good spectral purity due to the Σ-Δ modulation which provides high-pass filtering of the phase noise. Technologies of different domains must be combined in order to design and build equipment configuration able to fulfil the identified targets and goals. The combination of the following technologies will be the substrate to achieve the development targets:

- Gallium Arsenide MMICs
- Silicon RF IC (for miniaturisation of intermediate frequency circuit and frequency synthesizer loop)
- Digital Signal Processing and advanced CMOS VLSI technology
- Advanced packaging techniques (MCM, LTCC)

II.ELECTRICAL DESIGN:

A high-level functional block diagram of the command receiver is given in Figure*.1*. The receiver analog section includes the pre-selector filter, the 30 GHz front-end, the first IF conversions and the L.O. signal generation section. The signal after low noise amplification and image band rejection is down-converted to an intermediate frequency; the signal plus noise power level is controlled by an analog non-coherent 2nd order AGC which avoids saturation along the receiver chain and clipping in the A/D converter process. A Preselect filter is located in front of the receiver in order to prevent it from being degraded in presence of out-of band spurious signal .

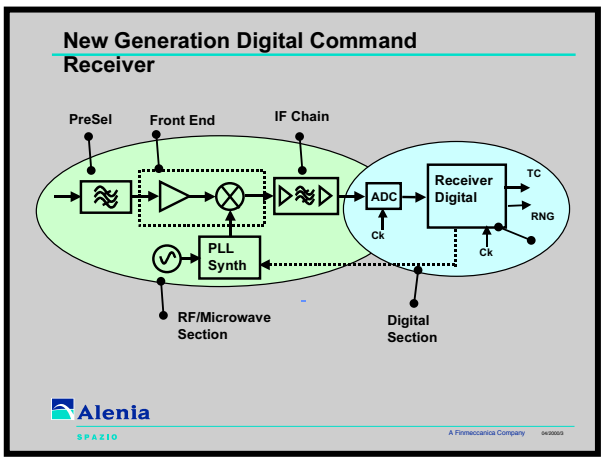


Figure 1: Receiver Block Diagram

The **Ka Band Front End** is based on the integration of gallium arsenide MMICs implementing the Low Noise amplification, the I/Q image rejection mixer and the times three multiplier. The LNA MMIC uses a three stages configuration with inductive source feedback to have at the same time low noise and optimum input matching within a 14 - 32 GHz bandwidth. The MMIC (figure 2b) also provides more than 20 dB gain. Each stage is self biased to reduce the performance

variations with the temperature. PHEMT GaAs 0.25um gate length technology is used with typical gm of 500mS/mm and cutoff frequency of 50 GHz. The MMIC LNA gain and noise figure is shown in the figure 2. In this specific application a very low noise figure, like in the communication payload receivers, is not strictly required while a fully integrated design is preferred in order to strongly reduce the production tuning effort and the final equipment cost. The LNA MMIC for this reason is directly used as front end first stage.

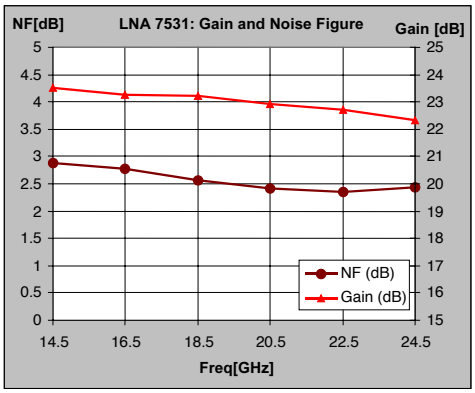


Fig. 2: 30 GHz LNA Gain and noise

The Ka band receiver front end (fig.3) provides a gain of 40dB, a noise figure less than 3 dB and an image rejection of 20dB (figure 4).

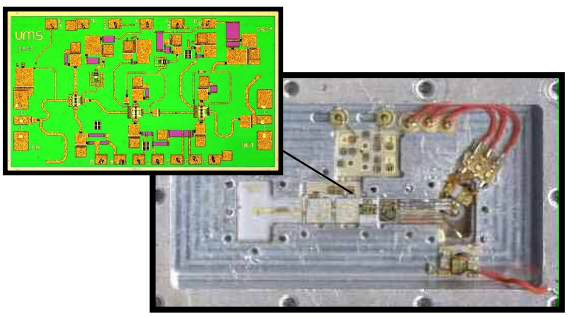


Fig. 3: 30 GHz Front End Hybrid

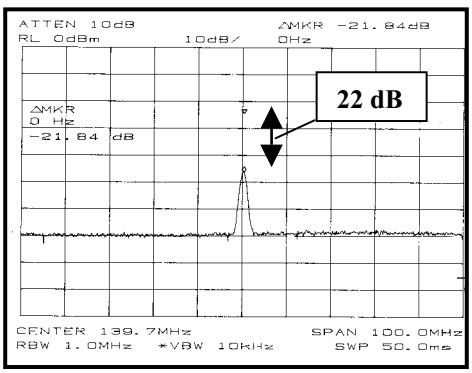


Fig. 4: 30 GHz Front End Image Rejection

The Front-End hybrid housing is designed in Silicon Aluminum material, that has the advantage of light weight, high thermal conductivity and a TCE compatible with LTCC.

Next integration step is the design of GaAs multifunction MMIC integrating the complete front end function in a single chip. A fully qualified GaAs PHEMT 0.15um process has been selected for this integration, it allows to achieve remarkable noise figure performances and to achieve a full integration with very significant cost reduction.

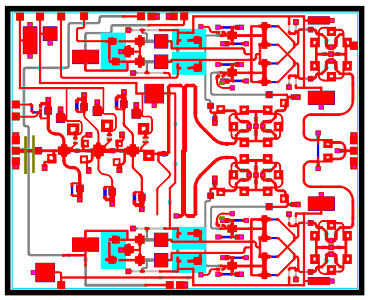


Fig. 5: Ka band/IF MFMMIC Front End Layout

The **IF amplifier chain** (140 MHz) has a gain of about 90 dB and has been realised with discrete cascode amplification stages and gain controlled amplifiers integrated in a silicon RF IC [2]. A SAW filter performs the proper filtering function while the gain control is used to realize the wideband analog AGC function. The input stage amplifier (input IF section) is designed in cascode configuration. The SAW Filter follows this stage and it guarantees 50 dB out of band rejection. The following IF amplifiers are integrated in the IF strip Analog ASIC. The control gain circuit (AGC) is implemented with a current subtraction system. The output Buffer is a 15dB gain amplifier, that guarantees the required output 1dB compression point. The control loop is composed by a detector and a comparator and it assures the 0 dBm output S+N power.

The complete IF receiver chain (more than 100 dB controlled gain in the deep space transponder version) has been realised with two complex LTCC trays. This technology approach allow to implement a full surface mount technology with significant improvement in the production lead time and remarkable cost reduction compared to standard technologies for flight hardware.

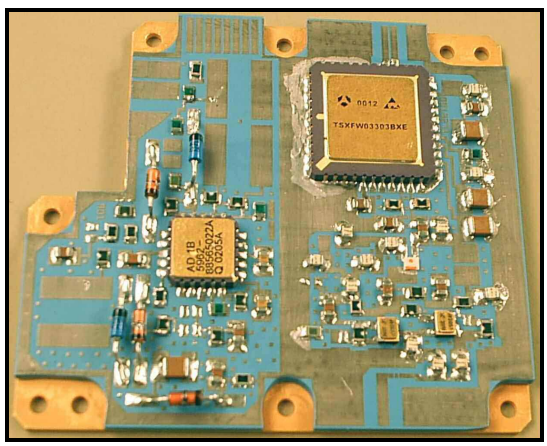


Fig.5: LTCC IF Amplifier Chain

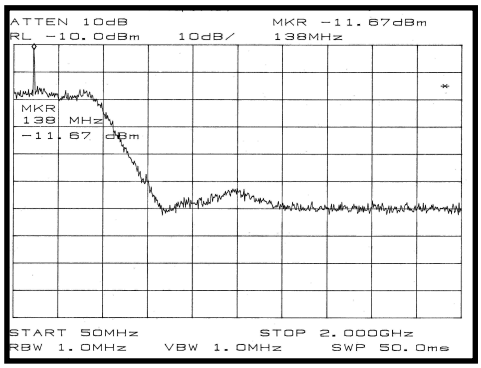


Fig.6: IF Amplifier Chain: Output Spectrum

The **LO Generation Circuit** provides a synthesised output frequency starting from a reference signal, coming from the TCXO (Thermal Compensation Xtal Oscillator, figure 7). The TCXO circuit is composed of a basic oscillator and of a analog compensation network which provides a frequency stability over the full temperature range of 1 ppm peak-to-peak of ±4 ppm over life. The compensation scheme uses a thermistor with multi-order resistive network.

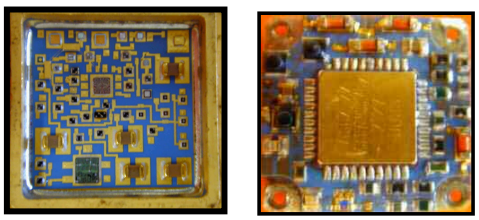


Figure 7: TCXO circuit

The heart of the LO generation circuit is a single chip fractional synthesiser that includes the programmable PLL functions. The synthesizer includes a dual-modulus prescaler capable of operating at input frequencies up to 3GHz, a third-order MASH modulator that controls the modulus of the prescaler, counters programming with serial and parallel data and a phase detector and charge pump. The synthesizer has been implemented in a 0.5u CMOS technology. The CMOS on sapphire technology is variation of silicon-on-insulator (SOI) technology. The greatest asset of this technology lies in the combination of high-performance RF, mixed signal, passive elements, and digital functions on a single chip. The synthesiser provides the coarse steps (integer) while the ΔΣ modulator the fine resolution to fill the gaps between the coarse steps (decimal). If we look at 1kHz-10kHz phase noise performances, that is the range in which the contribution of the synthesiser is the most important, there are no differences in performances due to the introduction of MASH circuitry. The measured phase noise performances are (fig.8b) very closed to the theoretical value.

The Chip internal schematic is shown in the following block diagram (figure 8)

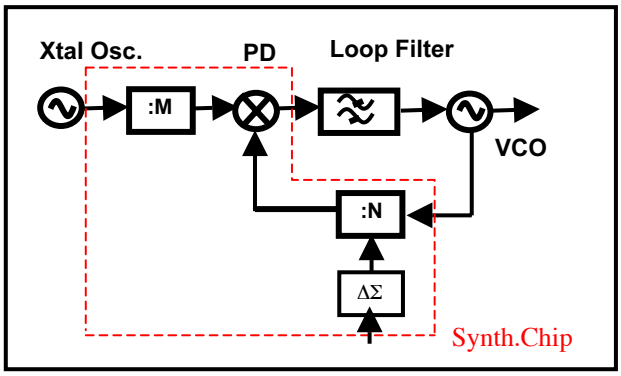


Fig. 8: Frequency Synthesizer Chip Block Schematic

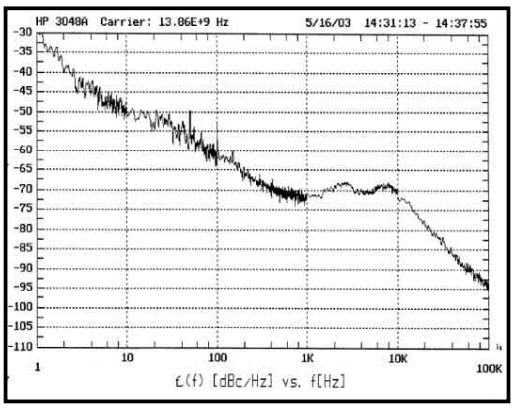


Fig. 8b Ku Band Loop Phase Noise Measurement

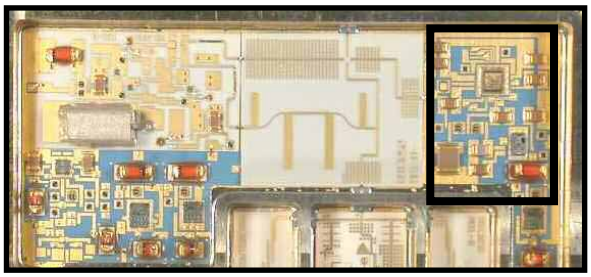


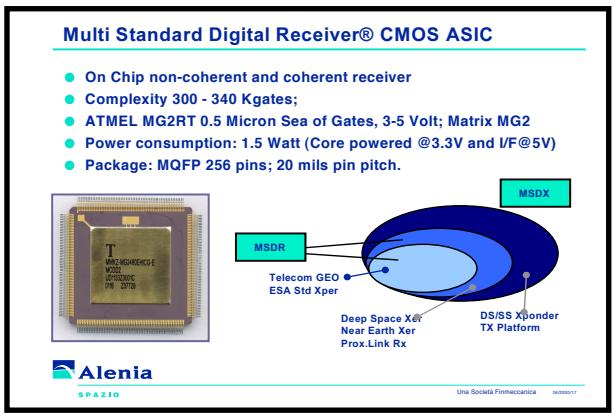
Fig.9: Integrated LTCC PLL Fractional Synth.

The progress of digital signal processing techniques and the improvements of the Very Large Scale Integration (VLSI) technologies allows the implementation of complex demodulation functions in digital domain and using advanced CMOS VLSI processes in a single-chip device (Multi-Standard Digital Receiver). The presulting architecturla and techonology solution leads to a very compact equipment, supporting both Frequency Modulation (FM), Phase Modulation (PM) and digital modulation, including spread spectrum, TT&C standards.

According to the high level receiver block diagram, figure 1, the receiver front-end performs the low-noise amplification, image rejection filtering and up-link signal down-conversion to the intermediate frequency. An analog wide-band AGC is implemented to keep constant the signal plus noise power at the ADC input, in order to minimise the quantization noise and saturation noise arising from the analog-to-digital conversion. The ADC is clocked at 43 MHz and the under-sampling approach is used for signal digitisation.

The digitised samples are passed to the Multi-Standard Digital Receiver CMOS ASIC for carrier recovery and data demodulation. According to the signal modulation format, useful power and data rate, the signal processing functions are programmed by means the customised embedded Minicontroller.

The FM demodulator is based on a *all-digital* delay-line detector and it employs an Automatic Frequency Control (AFC) loop in order to keep the up-link signal at the center of the receiver channel. The AFC loop detector exploits a classical quadrature correlator which controls the LO frequency generated by the Fractional-N synthesiser. The PM demodulator uses an *all-digital* carrier recovery loop which can be configured to cope with up-link signal having large dynamic and frequency change rate, due to combination of advanced signal processing techniques (second-order/third-order loops, on-board aided acquisition) and dedicated digital design solutions (CORDIC phase rotator, programmable loop filters). Finally, the data demodulation is accomplished by a Costas loop for command subcarrier demodulation and by a Data Transition Tracking Loop for bit synchronisation purposes..



A gate complexity of about 300 kgates is needed to relaize in a single chipp all the receiver functions. A standard 0.5 um CMOS process has been used to realise the CMOS ASIC.

III.TECHNOLOGIES:

The described receiver has been designed using state of art space technologies for what concerns the semiconductor devices and the interconnection an packaging techniques. The combination of different processes allows to obtain a significant technology improvement with respect to actual space products making use of the following technology doamins:

- GaAs MMIC multifunction for the microwave section
- CMOS SOS for the frequency synthesis
- Si Bipolar RF IC for the RF/IF functions
- Digital CMOS VLSI for the digital receiver platform

As concerns the interconnection and packaging the receiver is designed making large use of LTCC (Low Temperature Cofired Ceramic) substrate for both hybrid and not hybrid sections. The MCM (Multi Chip Module) hybrid section mounts components as bare dice, while the not hybrid section the packaged ones. This technology is able to provide cost-effective hardware solutions suitable for high volume manufacturing. The LTCC allows to reduce the concept time in the engineering phase offering significant advantages also in the production phase. It is capable of complexities up to systems in a package and has been demonstrated to be competitive in terms of excellent high frequency performance, high power handling, innovative compact 3D structures and, thus at the end, miniaturization. The LTCC offers a challenge due to a reduction contacts/transitions number, increasing of reliability due to less interconnects; cost savings - fewer steps required for component integration, a large number of assembly steps are eliminated; density/space savings - by embedding the components in the substrate layers, the footprint constraints are removed and enhanced electrical performance. Electrical isolation between supply and RF lines in the ISP ceramic substrate is done by internal ground planes.

IV.CONCLUSIONS

Even if the receiver is composed of five different sections, what is innovative is the technological continuity and the high integration factor. This is the first step for a system-in-package (SiP) approach. The creation of an integrated design enviroment that supports the componets routing increases the design efficiency of system architecture. To avoid the coupling between the different circuitry and possible self oscillation for example in the IF section, which manages about 100dB gain at the same frequency, the different sections will be shielded using a mechanical frame screwed in the substrate down to the mechanical housing. The MCM is a common carrier onto which different IC are mounted. The evolution of this approach will be the system-on-chip (SoC) receiver making use of avanced RF CMOS processes for most of the system and integrating over the silicon substrate the required GaAs chip with flip chip technique.

V. REFERENCES

(1) M.C.Comparini “Microwave Technology for space application: a fast evolution to be competitive”-*European Microwave Week 2000,* Paris, October 2000

(2) F.Adirosi M.C.Comparini, C.Leone “Application of silicon based RF IC devices in space communication systems & equipment”-*European Microwave Week 2000,* Paris, October 2000