Integrated receiver components for low-cost 26 GHz LMDS applications using an 0.8 μm SiGe HBT technology

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***Abstract*— The authors have demonstrated integrated receiver components addressing 26 GHz *L*ocal *M*ultipoint *D*istribution *S*ervices (LMDS) applications using a standard SiGe HBT MMIC process with an layouted emitter width of 0.8 μm. Compact circuit layout and transistor structure optimization are applied to a mature Si/SiGe technology, resulting in low-cost integrated circuits enabling consumer-oriented systems at 26 GHz.**

The integrated receiver components are a downconverter and a static 2:1 divider. The downconverter IC consists of a preamplifier and a mixer with an IF buffer. The conversion gain is determined to be 24 dB for an intermediate frequency of 200 MHz, and the maximum frequency of operation for the divider is 28.2 GHz.

I. Introduction

The emergence of *L*ocal *M*ultipoint *D*istribution *S*ervices will open up an additional mass market for rf-systems. In contrast to the 3.5 GHz band, the 26 GHz band has the disadvantage of the necessity of line-of-sight. This disadvantage at the first glance makes the reuse of the valuable frequency-bands possible by designing well defined pico-cells leading to the need of low-cost system components. SiGe HBTs meet the need for advanced microwave performance with relaxed lateral scaling[1], providing cost saving potential. Wafer-level packaging, which has been prototyped in [2], provides low-cost solutions.

This paper will demonstrate an integrated downconverter and a static 2:1 divider realized for 26 GHz LMDS applications using HBTs in a commercially available Si/SiGe HBT MMIC process.

II. Technological features

The basic for the integrated circuits discussed in this paper is the second generation [3] of the commercially available Si/SiGe HBT technology with three metalization layers at ATMEL Germany GmbH [4], [5]. The devices feature a high and constant Ge mole fraction in the base layer leading to an efficient hole-blocking valence band barrier at the base-emitter interface. The new SiGe2 process introduces shrunk lateral dimensions, a thinner and higher doped base layer, an L-spacer technology instead of LOCOS, and reduced parasitics to increase transit frequency f_T and maximum frequency of oscillation f_{max}. The process does not use trench isolation for the devices. For transistors with an layouted emitter width of 0.8 μm (effective: 0.5 μm), the transit frequency f_T is 50 GHz, typically. Two different collector doping profiles selectable for each individual transistor by a selective collector implant, the transit frequency can be increased to 80 GHz. For all circuits shown here, substrates with a resistivity of 20 Ωcm are used.

The 0.5 μm emitter transistors have been modified by introducing interdigital base and collector electrodes. The effect of these modifications on the rf performance have been analyzed. The individual transistor layout structures are depicted in Figure 1.

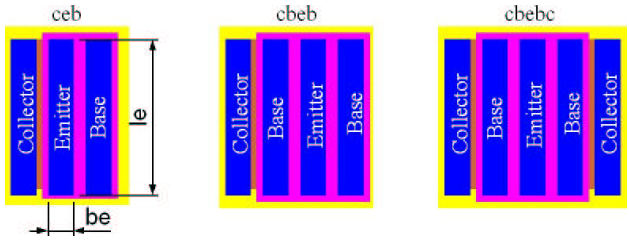

Fig. 1. Electrode configuration of the investigated transistor structures, $b_e \times l_e = 0.5 \times 19.7\ \mu m^2$ (effective)

Transit frequency and maximum frequency of oscillation values are extracted from data after de-embedding the pad parasitics. Here, values for f_{max} are extracted from maximum available gain (MAG). The individual extracted highest values have been obtained at a current density of $\approx 1.7\ mA/\mu m^2$ and are assembled in Table I.

	f_T/ GHz	f_{max}/ GHz
ceb	80	55
cbeb	75	70
cbebc	75	75

TABLE I
TRANSIT FREQUENCY AND MAXIMUM FREQUENCY OF OSCILLATION OF THE DIFFERENT TRANSISTOR STRUCTURES

The transistor layout configuration with the best rf performance for $b_e \times l_e = 0.5 \times 19.7\ \mu m^2$ is the "cbebc" one. This transistor configuration has been taken to set up a scalable MEXTRAM model, as described earlier in [6]. The scalability is refered to the number of emitter-fingers and to the lenght of the fingers.

III. Downconverter

The layout of the integrated downconverter for 26 GHz can be seen in Figure 2, which combines a preamplifier with a single-ended input, a Gilbert cell mixer with a single-ended

LO-drive input and a differential output intermediate frequency buffer amplifier circuit. The topology of the circuits have been adopted from [7]. The modifications are described in the following subsections.

To keep the layout compact, the reactances and matching networks have been realized using lumped elements (MIM capacitors and spiral inductors). Transmission lines with non-negligible length in the layout are taken into consideration by models using a quasi-thin-film microstrip approach.

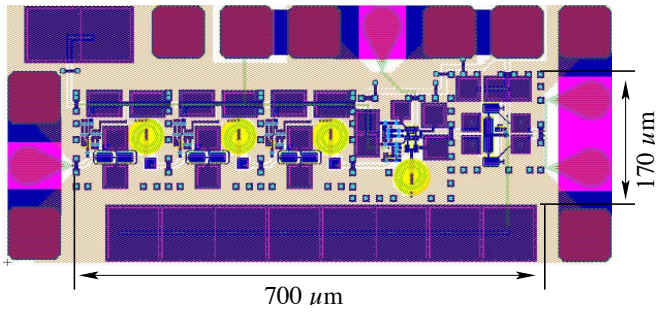

Fig. 2. Layout of the downconverter at 26 GHz $\left(700 \times 170\,\mu\mathrm{m}^2\right)$

A. Preamplifier

The preamplifier is a three stage amplifier in cascode configuration, with identical stages depicted in Figure 3. The biasing is realized by a slightly modified current mirror with a separate reference voltage supply and a resistive voltage divider, respectively. Inter-stage matching is achieved by the L-C-network. A two turns inductance with $\mathrm{L} = 0.15\,\mathrm{nH}$ in the third metalization layer has been used. Taken from measurements, the quality factor calculated from the Y_{11}-Parameter is $Q = 11$ at the design frequency of 26 GHz.

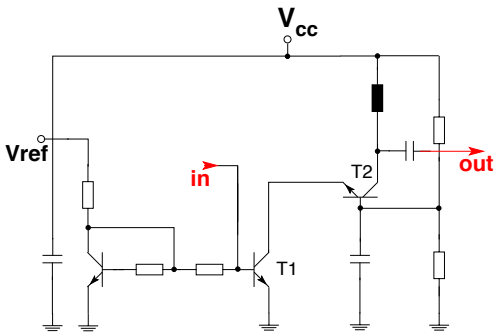

Fig. 3. Circuit schematic of one single stage of the preamplifier

The preamplifier circuit part, which is the left part of Figure 2, has been realized separately with its own contact pad configuration. Based on the design in [7], the preamplifier has been layout-optimized (10% layout-size reduction), tuned to the higher design frequency and the DC power consumption has been reduced.

On-wafer S-parameter measurements have shown that in a $50\,\Omega$ test environment the amplifier provides a maximum gain of 20.0 dB at 25.6 GHz (see Figure 4). The noise figure, for which this circuit has not been optimized, yet, has been measured to be $\mathrm{NF}_{50} = 8\,\mathrm{dB}$.

The DC power consumption of the preamplifier is 42 mW at 3.0 V supply voltage.

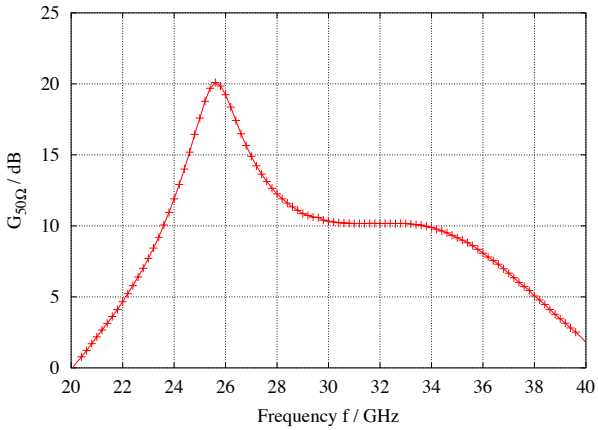

Fig. 4. Gain of the preamplifier in a $50\,\Omega$ test environment

B. Double balanced mixer

The topology of the mixer is a slightly modified Gilbert cell configuration, buffered by an emitter follower stage (see schematic in Figure 5).

The mixer is supplied single-ended with the RF signal at the lower transistor and with the LO signal at the upper transistors of the Gilbert cell. The complementary inputs of the mixer are shorted by capacitors.

The usual transistor current source in the mixer core is replaced by a spiral inductor of two turns. This replacement allows to reduce the voltage level at the collector of the switching transistors in the Gilbert cell by the voltage needed for a transistor current source, increasing the output linearity. The main reason for this replacement is the poor performance of a transistor as a current source at 26 GHz.

The differential IF output of the Gilbert cell is filtered by an RC filter with a corner frequency of 1.5 GHz and buffered by an emitter follower, which has a transistor current source as a load. Based on the design in [7], the output linearity has been increased.

The DC power consumption of the mixer is 78 mW at 3.0 V supply voltage.

C. System characteristics

The downconverter presented in Figure 2 is characterized on-wafer. The single-ended RF and LO ports have been driven by external signal generators. The downconverted IF signal has been detected by a spectrum analyzer. The single-ended conversion gain, shown in Figure 6, is measured by keeping the IF constant with $f_{RF} > f_{LO}$. The complementary IF output port has been terminated during the measurement with a $50\,\Omega$ load, externally. The highest conversion gain obtained in the single-ended measurement configuration is 21 dB. The differential conversion gain of the downconverter can be calculated to be 24 dB. With $f_{RF} > f_{LO}$ and $f_{RF} < f_{LO}$, the identical conversion behavior has been observed. The IF output power level for the two complementary output port were identical within the measurement accuracy of 0.5 dB.

In Figure 7 the conversion gain as a function of the RF power is presented. The $-1\,\mathrm{dB}$ input compression point is determined to be $\mathrm{P}_{-1\,\mathrm{dBm,in}} = -24\,\mathrm{dBm}$. The correlating -1 dB output compression point is $\mathrm{P}_{-1\,\mathrm{dBm,out}} = -6.2\,\mathrm{dBm}$.

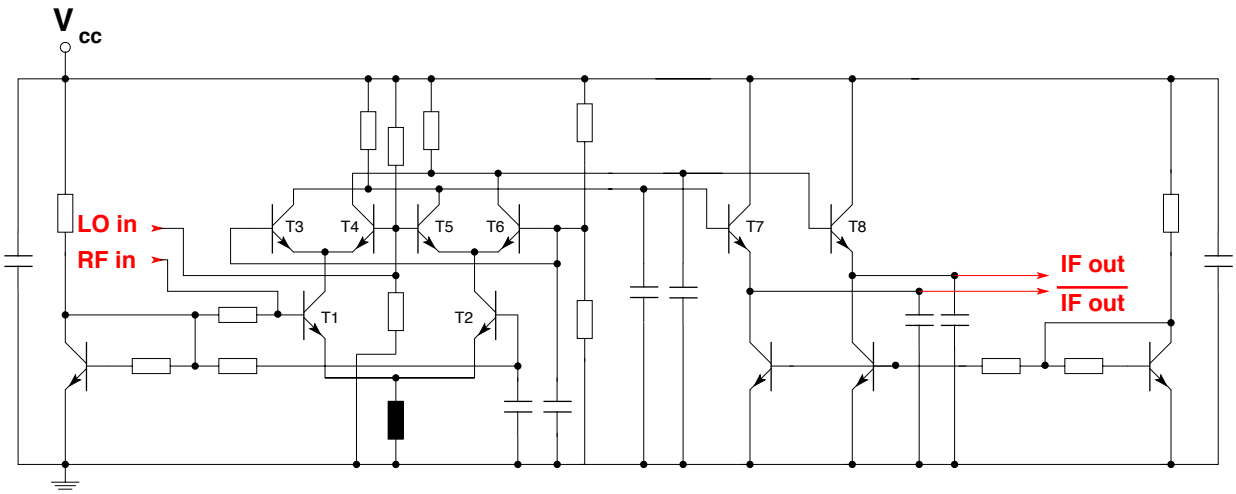

Fig. 5. Circuit schematic of the mixer circuit part

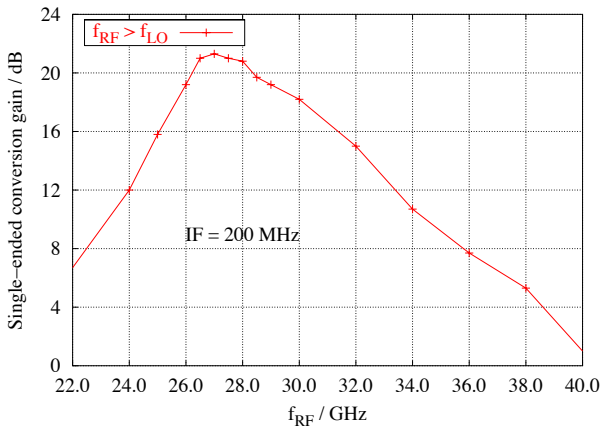

Fig. 6. Single-ended conversion gain of the receiver at a constant IF of 200 MHz

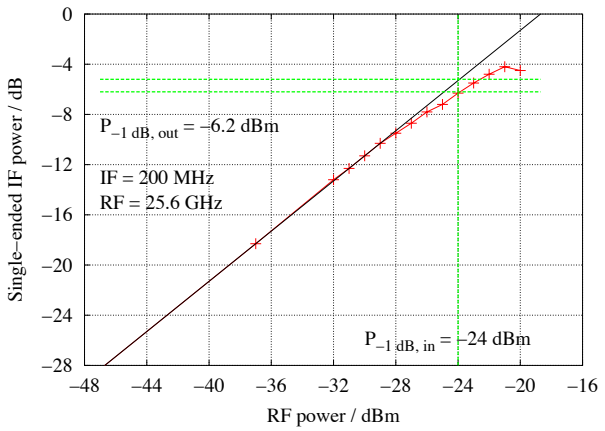

Fig. 7. Input and output -1 dB compression point of the conversion gain at RF = 25.6 GHz and IF = 200 MHz

The overall DC power consumption is 120 mW.

IV. Static 2:1 Divider

The static divider is based on the master-slave flip-flop approach consisting of two D-latches. The output of the second latch is fed back to the input of the first latch. In Figure 8 the divider circuit is depicted, implemented in standard Emitter-Coupled-Logic (ECL).

For a simple on-wafer measurement setup, the complementary input port has been short-circuited to ground by a capacitor. The inverted output port is terminated by an on-wafer 50 Ω resistance. The remaining input and output ports are contacted single ended by ground-signal-ground pads, like depicted in Figure 9. The divider consumes a chip-area of $100 \times 100\ \mu m^2$, defined by minimum device and metal distances.

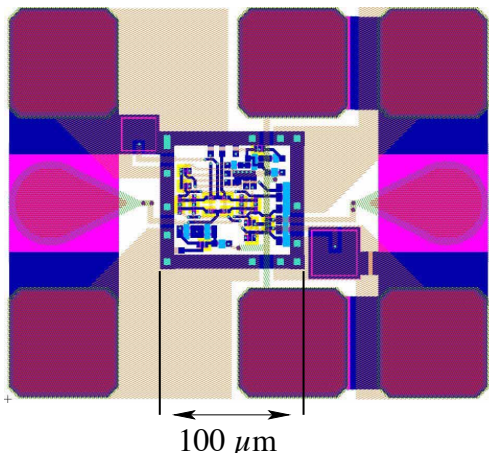

Fig. 9. Layout of the static 2:1 divider $\left(100 \times 100\ \mu m^2\right)$

The divider has been characterized on-wafer, driving the single-ended clock-port by an external signal generator. The divided signal has been detected by a spectrum analyzer. The input power sensitivity can be seen in Figure 10.

The upper operation input frequency limit has been determined to be 28.2 GHz at a power-level of 7 dBm at the input. Around the design frequency of 26 GHz the minimum input power is about −6 dBm. The DC power consumption is 88 mW at 4 V supply voltage.

V. Conclusion

A standard commercially available SiGe HBT process has been used to design and fabricate a downconverter, consisting of a preamplifier and mixer, using area-efficient design techniques, which avoid distributed elements. For the design, layout optimized transistors have been used. The

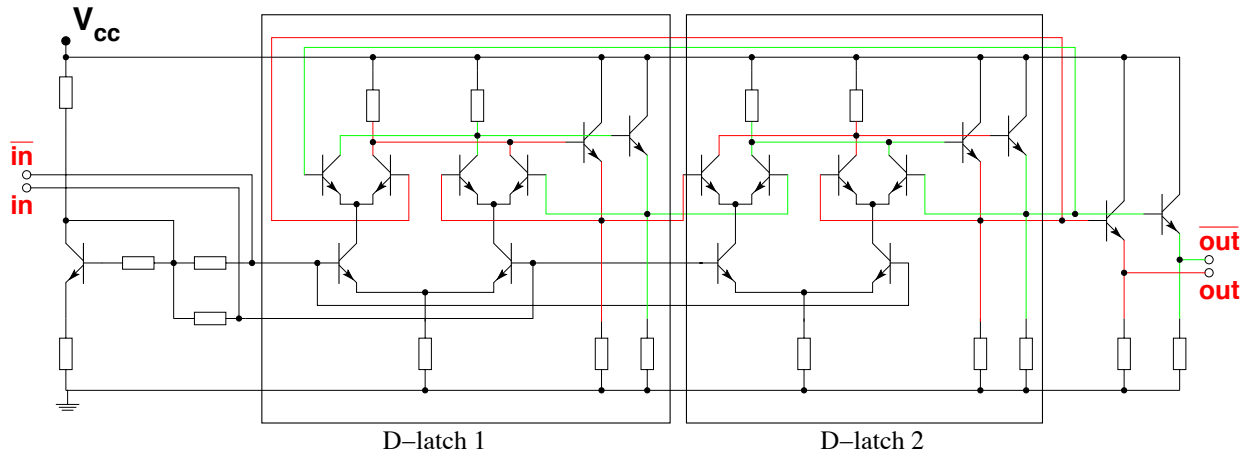

Fig. 8. Circuit schematic of the static 2:1 divider

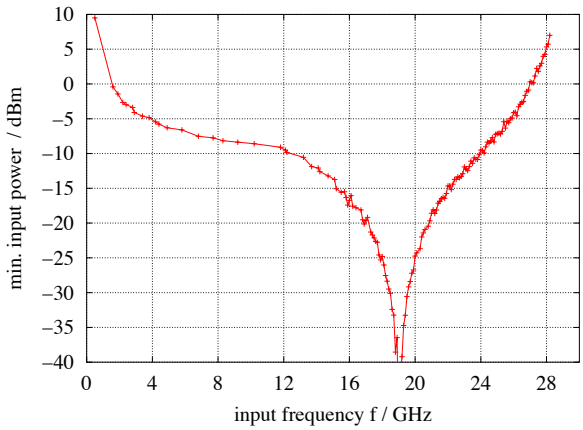

Fig. 10. Input sensitivity for the static 2:1 divider

conversion gain of the downconverter has been obtained to be 24 dB. The static 2:1 divider operated up to 28.2 GHz.

It is expected that these prototyped receiver components can be used in short-range communications (WLL, LMDS) aimed to the consumer mass market.

Acknowledgment

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