High-Performance Integrated RF-MEMS: Part 1- The Process

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***Abstract* — RF MEMS have been pursued for more than a decade as a solution to high-performance on-chip fixed, tunable and switchable passives. However, the implementation of RF-MEMS into products has remained elusive. This is partly due to special-purpose processes that only supported a narrow application field, in many cases optimized for single devices. This prevented aggregation of volumes to justify the manufacturing infrastructure of even a single production foundry. This paper presents a single process that has been implemented in multiple foundries and highlights a wide range of high-performance devices including switches, inductors, varactors, and phase-shifters that have been or are being built using this process. This process thus forms the foundation for a wide range of reconfigurable and tunable RF passive circuits.**

I. Introduction

RF-MEMS holds great promise for improving performance and increasing the integration of the RF front-end of wireless systems. Many high-performance devices have been built using RF-MEMS including shunt and series switches[1]-[3], variable capacitors[4,5], inductors[6,7], and low-loss and variable transmission lines [8]. However, these devices were developed in processes customized to build individual device types or were built in captive foundries. The resulting narrow range of applications will not generate the volumes needed to justify the required foundry capital investment nor even that needed to stabilize the process itself to provide high yields. While some standard processes exist [9,10], they are unsuited for RF applications due to their resistive materials.

High performance passives are usually needed in groups within a RF sub-system, such as in tunable filters, filter banks or in phase shifters. A process suitable for integration must be able to build all of these in one chip where each of the devices maintains its high performance and where the various devices can be interconnected with high Q to maintain the high performance of the overall circuit. Another drawback to existing technology has been the required high temperature processing that limited monolithic integration with active circuitry such as amplifiers or VCOs. This paper presents details of a flexible manufacturing process flow that addresses these shortcomings and outlines design and measurements of high-performance devices created in the process.

II. Materials

RF-MEMS requires high quality metals and insulators for state-of-the-art well-controlled RF characteristics. All of our materials needed to have the following properties:

- Low deposition temperature (<300 C) to allow post-processing on CMOS
- High etching selectivity
- Low stress and stress gradients
- Precise patterning techniques
- Available inter-layer adhesion layers

The first consideration is the choice of MEMS structural material. We use an insulator for this purpose to provide high electrical and RF isolation between actuation and RF sections of the devices. To provide electrical contacts and electrodes for electrostatic actuation, conducting surfaces are formed on portions of this structural insulator. Thus our MEMS structures typically consist of sections that are composed simply of just an insulator and other sections where there is a tri-layer sandwich of conductor-insulator-conductor that is balanced to manage the intrinsic stresses.

The sacrificial material has been chosen to provide uniform smooth layers, good step coverage, rapid complete removal from thin gaps, formation of stacked patterned layers for vertical topography and additional functionality when intentionally protected from release etch.

There are three basic applications of metal in RF-MEMS: buried conductors, exposed electrodes, and electrical contacts. The key factor in choice of interconnect metal is low resistance. The lowest resistance metals are silver, copper, and gold. Silver, which has the lowest resistivity, is limited by relatively high diffusion rate and susceptibility to corrosion in likely chemistries. Gold is limited by available processes for thick patterning and planarization and has significantly higher resistivity. Thus our choice of copper for the buried conductors was driven by:

- High layer conductivity (> 4 x 10^7 S/m)
- Corrosion resistance to processing steps
- Rapid deposition of thick (>3μm) layers
- Available mature CMP processes

Since electrodes and electrical contacts are both exposed to the ambient, we have chosen to use the same metal for both. Our choice of Au-based metal was driven by:

- Low contact resistance (<0.5 ohms)
- Low required contact force (<200μN)
- High melting temperature (>800C)
- Low self-adhesion
- Low catalytic activity

The choice of insulators was constrained by :

- Low loss tangent (<.003) and DC conductivity
- Low dielectric constant (<5)
- High breakdown field
- High mechanical yield strength
- Rapid deposition of thick (>3μm) layers
- Available mature CMP processes

Insulators considered included alumina, high-resistivity silicon, silica, various polymers and GaAs. High-resistivity silicon was eliminated due to the difficulty in maintaining high-resistivity of exposed surfaces during subsequent processing, the required high processing temperatures and high dielectric constant. GaAs was avoided due to the cost of the deposition, its toxicity and high dielectric constant. Polymers were considered unsuitable due to their poor yield strength. Alumina fulfilled everything except for its high dielectric constant. Silica fulfilled all of the necessary requirements and also had immediate process availability within the candidate foundries.

Another consideration is the choice of substrate. We chose to make the process relatively substrate independent. Thus we can fabricate high-performance passives, switches and other MEMS such as tunable capacitors directly on top of functional electronic circuits, both passive and active, even on a resistive substrate such as provided by bulk CMOS. The complete range of compatible substrates is limited by thermal expansion, although these are not severe due to the low processing temperatures. All work to date has used low-resistivity (<10 ohm-cm) silicon substrates.

III. Process Flow

The nominal process stack is shown in Figure 1. The overall flow is divided into three main sections: substrate connect, thick metal and thin metal. The substrate connect layer is used to isolate the upper layers from the substrate, make high-quality electrical connections to underlying circuitry and provide a planarized surface for subsequent processing.

The thick metal section, used primarily for passives and interconnects, is composed of copper embedded in silica. This is built up in 7 μm thick layers composed of a nominal 3.5 μm sheet conductor and a 3.5 μm stud interconnect. Each layer is planarized using CMP. The nominal process uses two of these layers, yielding 14 μm of combinations of copper and/or silica, although more or fewer layers can be used to optimize performance/complexity/cost tradeoffs.

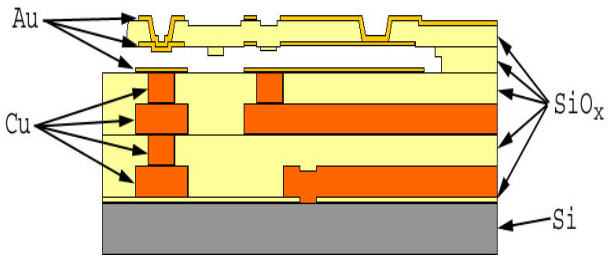

Fig. 1. Multi-Function MEMS Process Stack.

The thin metal section is composed of three layers of a gold alloy 0.5 μm thick that are used for electrodes and contacts, two layers of sacrificial material that are 1.5 μm and 0.5 μm thick respectively and a 2 μm silica mechanical layer The two thicknesses of sacrificial material enable the fabrication of mechanical dimples that are used for stiction reduction, mechanical stops, electrical standoffs and electrical contact bumps. The top two Au-alloy layers and the silica mechanical layer may be used together in structures to form tri-layers that are stress-balanced over a wide temperature range.

The process and material properties have been determined from test structure measurements and measurement extractions. These properties have been captured in CoventorWare™ for visualization and modeling of the 3D structure leading to straightforward electromechanical, damping and thermal simulations of various devices using CoventorWare™ and detailed RF analyses using Ansoft's HFSS™.

IV. Example RF Devices

A wide range of devices has been designed into this process and many others are in development. The most mature designs in the process are DC and RF switches. Details of these will be presented in a follow-on paper. Other designs include low-loss transmission lines along with variable and fixed capacitors and inductors. Circuits including phase-shifters and switchable filters have also been implemented.

	Strip Width, μm	Gap Height, μm
"E"-Line	11	10.5
"F"-Line	5	3.5

Table 1
Embedded microstrip designs.

As an illustration of the flexibility of this process, consider two simple 50Ω embedded microstrip lines created using different sets of the conductors in this process. The structures are dimensionally defined in Table 1. The E-line provides good overall RF performance and the deeply buried F-line enables high isolation DC-RF crossovers. Transitions from coplanar probe pads to each of the transmission lines were designed to provide good return loss without further de-embedding for on-wafer measurements. These pad transitions are also used directly in products. The line and the pad transition 3-D structures are shown in Figures 2 and 3.

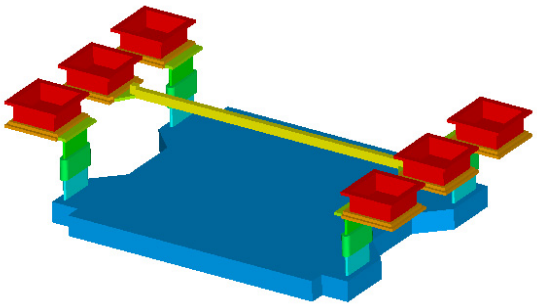

Fig. 2. E-Line 3D model including CPW pad transition with silica layers hidden and vertical dimension magnified 10x.

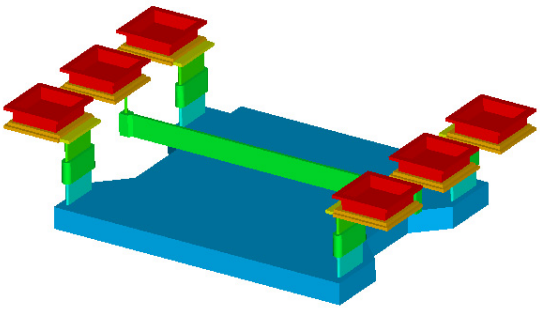

Fig. 3. F-Line 3D model including CPW pad transition with silica layers hidden and vertical dimension magnified 10x.

Figure 4 shows a fabricated 2mm by 2mm transmission line test die containing two line lengths, open-circuit and short-circuit test structures for both types of lines. A comparison of HFSS simulation results and calibrated on-wafer measured data for two lengths of these two transmission lines from a similar die are shown in Figures 5 and 6. The data and simulations shown fully include the effects of the coplanar pads for on-wafer characterization. Note that the simulations match the measurements closely and that the transmission line behavior is fairly ideal. However, most of the high-frequency losses do not scale with the transmission line length. This fixed excess loss originates in the coplanar pads where the fields are not shielded from low-resistivity silicon.

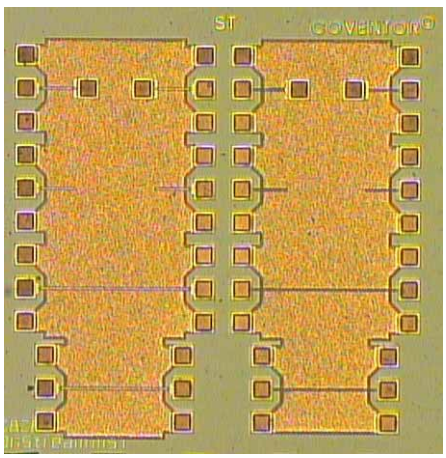

Fig. 4. E and F fabricated transmission line test structures.

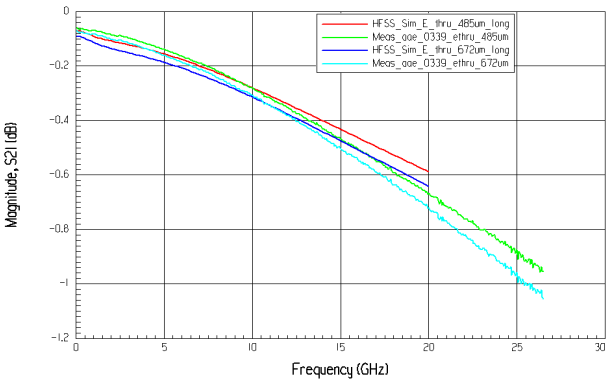

Fig. 5. Comparison of measured and simulated insertion loss for 485µm and 625µm lengths of E-Line.

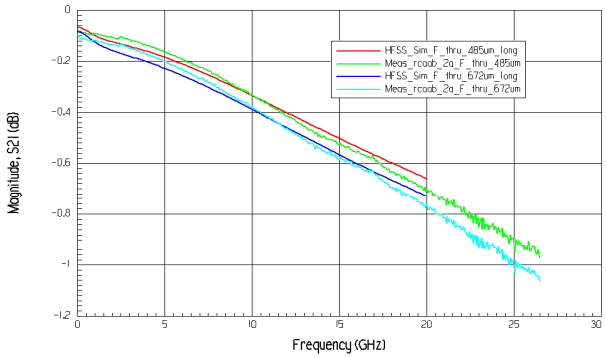

Fig. 6. Comparison of measured and simulated insertion loss for 485µm and 625µm lengths of F-Line.

The induced current density in the substrate is included in the 10 GHz simulation results shown in figure 7. Note that the substrate current is confined to a region near the pads. For devices operating below 5 GHz, the additional loss is negligible but devices operating at higher frequencies would benefit from an insulating substrate. De-embedding the pads yields a loss at 5 GHz of < 0.15dB/mm for the E-line and < 0.3 dB/mm for the F-line. At 26.5 GHz, this specific loss is < 0.4 dB/mm for the E-Line and < 0.5 dB/mm for the F-Line. Measured return losses are > 30 dB up to our measurement limit of 26.5 GHz. Other transmission lines designed in this process achieve losses of < 0.1 dB/mm at 5 GHz. These performances are unprecedented for high quality transmission lines on low-resistivity silicon substrates.

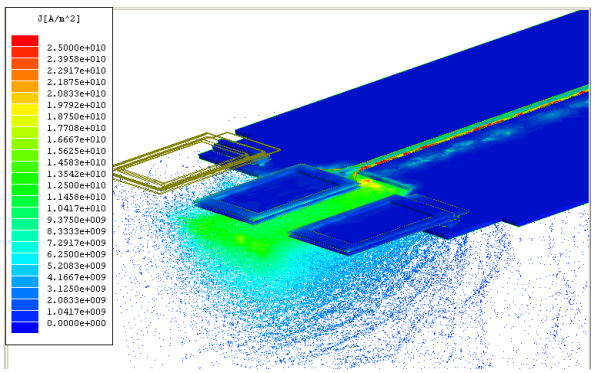

Fig. 7. E-Line HFSS simulation plot showing current densities in CPW pad transition.

Inductors of both stacked and planar geometries have also been designed and constructed in this process. The thick copper provides high Q at lower frequencies. The B5MLT symmetric balanced 2.6 nH inductor shown in Figure 8 demonstrates this concept with the close-up of the winding stack in Figure 9. The copper windings are 10.5 µm thick, which provides a Q of 12.6 at 3.5 GHz which is good for these low-resistivity silicon substrates. Inductors of value near 10 nH with Q of ~10 have also been designed and fabricated.

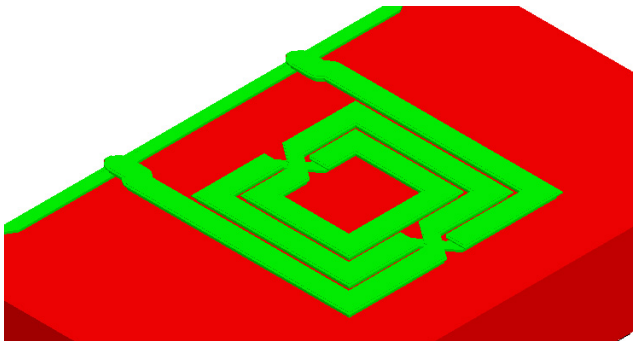

Fig. 8. Multilayer symmetric inductor B5MLT.

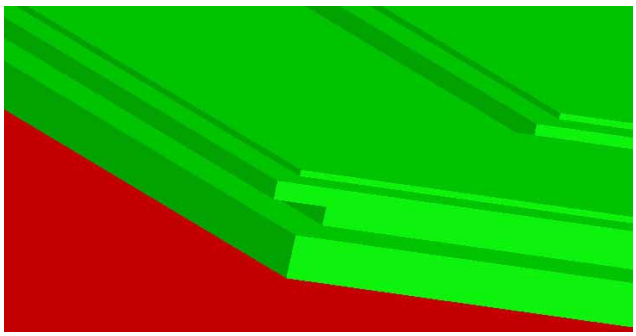

Fig. 9. Close-up of B5MLT windings.

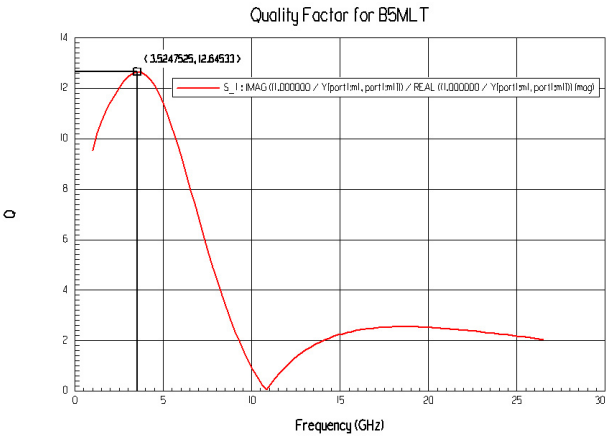

Fig. 10. Q determined for B5MLT.

Design details and measured performance of a range of other devices (e.g. switches, varactors, transformers, phase shifters, filters) and integrated circuits and sub-systems built within this process will be presented in future papers.

IV. Conclusions

This paper has presented a general-purpose RF-MEMS manufacturing process that has been implemented in multiple foundries. This process provides the necessary flexibility to simultaneously address a wide range of applications and device designs while at the same time providing the high performance expected from RF-MEMS. This approach is necessary to provide a mature, robust and cost-effective infrastructure for product development and manufacturing, such as is found in standard semiconductor process flows. It is also required for the integration of multiple MEMS devices to form products such as monolithic impedance-stable tunable filters. Transmission line and inductor examples were presented to illustrate the flexibility of and a flavor of the high RF performance achievable within this process flow.

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