An Original SiGe Active Differential Output Power Splitter for Millimetre-wave Applications

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Abstract — **This paper deals with an original design of an active power splitter featuring a differential output presenting a greatly enhanced even mode rejection. The proposed circuit consists in two cascaded common emitter and common collector differential pairs. For achieving the best performance, it is shown that each of these two differential pairs requires a specific common node to ground impedance that is discussed. The circuit has been implemented on a 0.25µm SiGe BiCMOS process and exhibits anticipated phase and amplitude broadband unbalance less than 6.5° and 0.6 dB respectively all over the 6-27 GHz frequency range. At 20 GHz, a common mode rejection ratio better than 43 dB is predicted, i.e. a maximum 0.12 dB /0.35° output signal unbalance.**

I. Introduction

Silicon-Germanium (SiGe) monolithic technologies are today very promising for future multimedia millimetre-wave applications, according to their ability to satisfy high performances, low cost and high integration trends. However, poor insulation properties of usual silicon substrates lead to low quality factor of interconnections and passive elements. As a consequence, although balanced circuit architectures are more attractive than single-ended ones in term of noise susceptibility, reduced EMI radiation and harmonic spectral quality, their silicon one chip integration suffers due to the lack of well performing passive or active structures for balanced signal generation or combining.

Reported silicon monolithic passive baluns [1-2] typically exhibit important loss levels, are not compatible with low cost CMOS/BiCMOS processes and they generally feature limited bandwidths. Moreover, they are not able to satisfy the high integration level required for multifunction chip design due to their large dimensions.

Therefore active baluns are an alternative since they offer better compactness. However, some of their electrical performances, i.e. noise figure, power handling capabilities and signal unbalance need to be carefully optimised in order to make them attractive. Different microwave active balun have already been reported, such as "common-gate common-source" circuits [3], distributed amplifiers based structures [4] and differential amplifier based circuits [5-7]. The first one exhibits very good performances but is narrow band while the second one features too large dimensions because of its distributed nature. Finally circuits using differential amplifiers cannot still achieve a well balanced operation, particularly as the frequency increases, as long as they are designed using the classical approach that employs a common node high impedance current source.

Nevertheless, among the different active balun topologies, the improved differential ones proposed in this paper can fit millimetre-wave applications requirements as it will be demonstrated.

After illustrating the limitations of the classical differential design, section II describes a method to overcome theses drawbacks. In section III, this method is applied to the design of a 20 GHz novel differential output power splitter. The circuit is implemented on a 0.25µm SiGe BiCMOS process from ST Microelectronics which allows good performances up to the low millimetre-wave frequency range. Some comments about our original layout, which involves some coplanar structures, are given in section IV. Expected performances are discussed in section V. Finally, a special care has been taken in stability analysis and is the subject of the last section.

II. Design Methodology for Millimetre-wave Differential Amplifiers

Usually, a high internal impedance current source and/or a parallel LC network is connected to the common node of differential structures in order to achieve even mode rejection. Nevertheless, as previously explained [8,9], the implementation of such a high impedance Z_{cp} cannot provide a sufficient well balanced output signal under high frequency operation. In fact, transistors of the differential pair feature capacitive output impedance that decreases with increasing frequency: therefore the high Z_{cp} is shunted through collectors loads, and becomes ineffective in the higher frequency range. This operation turns out into severely unbalanced performance. To overcome this problem, a method has been proposed for common-source FET differential amplifier configuration [8]. We have extended this technique to silicon bipolar differential amplifiers, including the three possible Common-Emitter (CE) Common-Collector (CC) and Common-Base (CB) transistor connections. Analytical investigations on these three configurations have been reported in [9].

For straightforward analytical developments, the differential amplifier schematic is split into a convenient set of two circuits resulting either from common and differential modes or from even and odd mode

excitations (figure 1). The first technique [10] leads to the common-mode rejection ratio (CMRR) calculation which is a very convenient criterion for unbalance quantification [11]. We have nevertheless used the second technique for the expression of the condition that leads to even mode cancellation. Thus, the four-port scattering parameters set is decomposed into a pair of two-port scattering matrices related to even and odd modes. A perfectly balanced operation can be obtained from even mode transmission cancellation (S_{21even}=0). By transposition from S to Z parameters, this condition becomes:

$$Z_{21_{even}} = 0 = Z_{21_{odd}} + 2 \cdot Z_{cp} \Leftrightarrow Z_{cp} = -\frac{Z_{21_{odd}}}{2} \qquad (1)$$

This expression means that an ideal balanced operation of a differential amplifier can be obtained by adequately synthesizing the Z_{cp} impedance [9] according to equation (1). This statement has been intensively employed in order to determine the nature of the Z_{cp} which has to be implemented on each of the two differential stages (CE and CC) of the differential balanced power splitter designed in the next section.

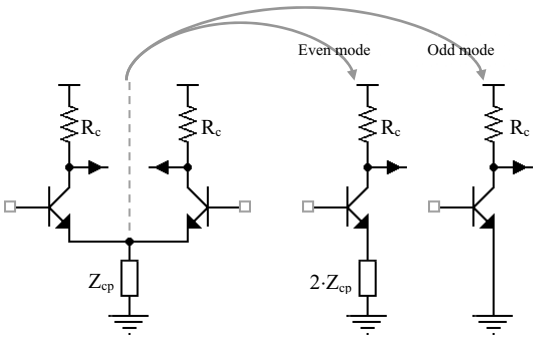

Fig. 1. Derivation of even and odd mode circuits of a differential structure.

III. Active differential phase splitter description

A. General description

The proposed power splitter, shown in figure 2, has been designed on the basis of the method previously described. It involves a cascade of CE (common emitter first stage between A and B) and CC (common collector second stage between B and C) differential pairs.

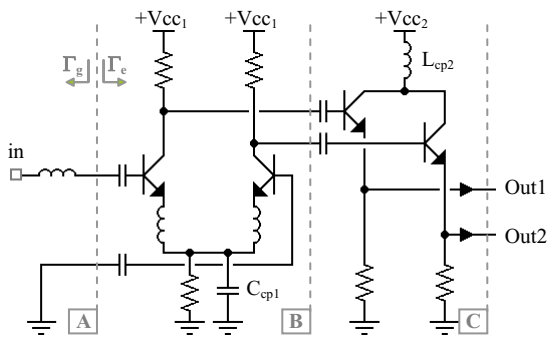

Fig. 2. Active differential output power splitter schematic.

The first stage sets the overall gain of the circuit. Dimensions and bias of the two input transistors, as well as their emitters' degeneration inductors, have been carefully optimized in order to achieve a minimum noise figure operation. Another inductor is serially connected at the input of the circuit in order to achieve broadband input matching. The choice of a capacitance C_{cp1} that connects the common emitter node to ground is very critical and is discussed in the next section.

The second stage provides an active broadband output matching for differential mode only. It plays a major role for the common mode rejection as highlighted below. The choice of an inductor L_{cp2}, which connects the collector common node to ground, is also very critical as discussed in the next section.

B. Optimal coupling impedance synthesis for each stage

Theoretically, the optimum Z_{cp} impedance obtained from the previous analysis for the CE differential amplifier is a serial association of a negative resistor and a capacitor [9]. It therefore requires an active circuit as the negative resistor [8]. Because of the complexity of this solution, this negative resistive part is omitted and Z_{cp} is made of a single capacitor. An extra parallel resistor is also needed for biasing purpose and adds an unwanted positive real part to Z_{cp}. Therefore Z_{cp} is far from optimum and the common mode rejection is only slightly improved with respect to the conventional approach that uses the resistor without C_{cp1}. Consequently, the CE differential configuration cannot fit lonely the high frequency performance requirements.

In order to solve this problem, the CC output differential structure is cascaded with the CE input one. Using the even mode transmission cancellation technique (Eq.1) for this second stage, it can be inferred that a single inductor is needed at the common node in order to synthesise a nearby optimal Z_{cp}. However, this optimal impedance is frequency dependant and the optimal inductor value decreases with increasing frequencies [9]. With a fixed inductance (L_{cp2}) a very high CMRR can be achieved but over a limited frequency bandwidth only.

IV. Layout considerations

The circuit has been implemented using a 0.25 µm SiGe BiCMOS technology from ST Microelectronics. The layout (figure 3) features a total area of 1050×670 μm^2 but the circuit itself is only 600×360 μm^2. A special care has been placed on designing the circuit very symmetrically because this point is very critical for an optimum high frequency well balanced performance.

Our design makes use of integrated silicon coplanar interconnections since, at considered frequencies, they display slightly lower losses than microstrip lines.

Moreover, microstrip based circuits often requires openings in the ground layer in order to interconnect resistors, transistors, inductors… Additionally this ground layer is made of the lower thin metal layer which enhances additional parasitic feedbacks effects due to its limited conductivity. Finally, it turns out that only a full circuit electromagnetic simulation is able to accurately predict the high frequency electrical performance of a silicon MMIC microstrip layout.

On the contrary coplanar interconnections are implemented using only the upper thick metal layer. Thus

ground openings are unnecessary and parasitic feedbacks are minimized thanks to the good conductivity of this ground plane. It turns into easier and more accurate simulations.

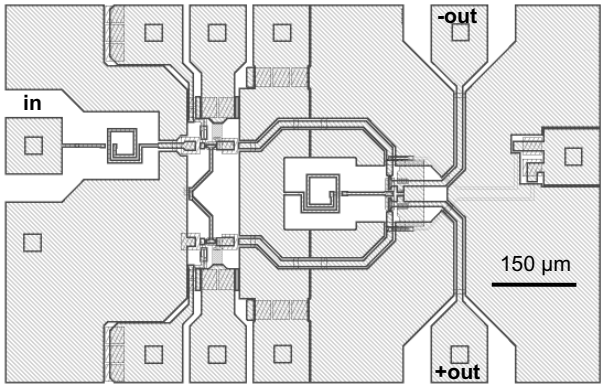

Fig. 3. The active differential power splitter layout.

V. SIMULATED PERFORMANCES

Simulated performances are obtained from electrical simulations performed with AGILENT ADS and EM simulations performed with ANSOFT HFSS. The impact of the circuit layout, including interconnections and various parasitics, is therefore fully considered. Simulated variations of the CMRR as well as the amplitude / phase unbalance of the active balun versus frequency are reported in figure 4 and 5 respectively.

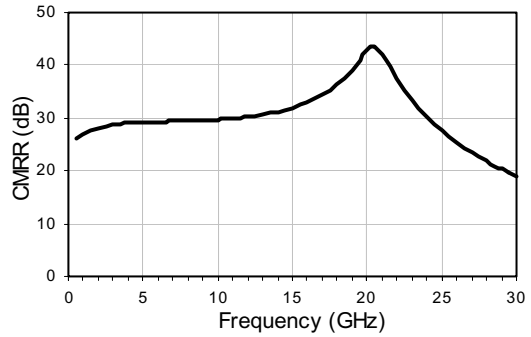

Fig. 4. Active differential splitter CMRR vs. frequency.

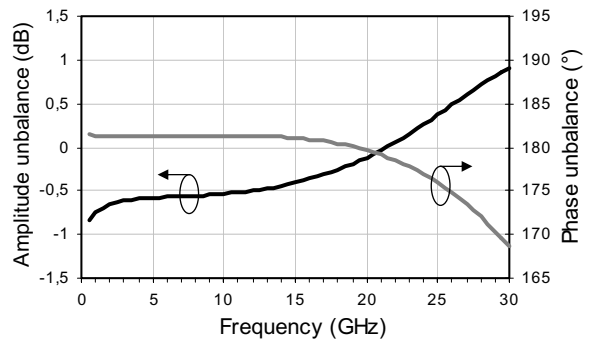

Fig. 5. Active balun amplitude and phase balance vs. frequency.

Figure 4 shows a CMRR better than 29 dB below 25 GHz. Normally the CMRR should severely deteriorate as the frequency increases due to the imperfect common node impedance of the CE input stage. In fact the output CC differential stage compensates for this anticipated degradation in the upper frequency range thanks to the inductor L_{cp2} at the CC common node. The value of L_{cp2} has been optimized in order to provide the best common mode rejection at 20 GHz which explains the 43 dB CMRR predicted at this frequency. One must notice that this CMRR peak only depends on the value of the inductor L_{cp2}. A maximum CMRR can therefore be reached at other frequencies (higher or lower) simply using different values for L_{cp2}, satisfying equation (1).

Supply voltage is made different for each stage with Vcc_1= 5.8 V and Vcc_2= 3.3 V. The first stage requires a larger supply voltage because of the bias resistor between ground and emitters of the CE differential pair. The value of this resistor results from a trade-off since it must be kept as high as possible for the best CMRR but must also be kept as low as possible for a minimum Vcc_1. The second stage doesn't need such a supply voltage since no resistor is needed between collectors and Vcc_2. The circuit output is not matched to 50 Ω and is designed to drive the RF port of a future double balanced mixer. Consequently, output matching and optimum linearity results from a trade-off between collectors' resistor loads, bias current and transistor geometry.

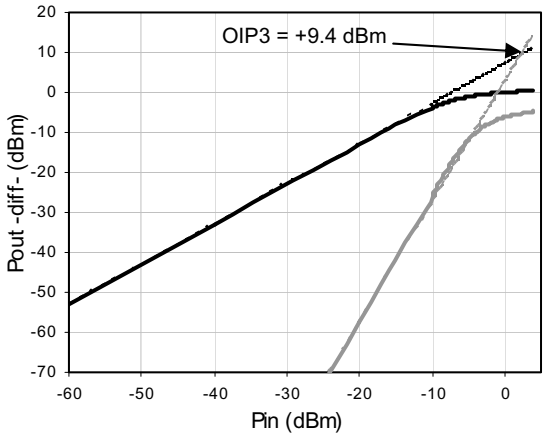

Fig. 6. Third order two-tone modulation curves related to differential output of the active balun.

Figure 6 displays the simulated third-order two-tone intermodulation versus frequency obtained for outputs loaded on the mixer input impedance. At the differential output, P_{1dB} is about -2.3 dBm and the intercept point IP3 is +9.4 dBm. The overall simulated performances are summarised in Table 1. The very large operating bandwidth over which a high CMRR is obtained is outstanding.

Broadband performances	
Frequency bandwidth ($\|S_{11}\|$ & $\|S_{out(diff)}\|$ < −10 dB)	6–27 GHz
Maximum balance error	6.5 ° / 0.6 dB
Minimum CMRR value	> 25 dB
Consumption	170 mW
20 GHz performances	
$\|S_{11}\|$	-13.2 dB
$\|S_{out(diff)}\|$	-12.0 dB

CMRR	43 dB
Balance error	0.35° / 0.12 dB
Differential gain	7.0 dB
Isolation	-28 dB
Noise figure	6.0 dB
Differential OIP_{1dB}	-2.3 dBm
Differential OIP_{3dB}	+9.4 dBm

TABLE 1
ACTIVE DIFFERENTIAL PHASE SPLITTER SIMULATED DATA.

VI. STABILITY ANALYSIS

Considering high internal reflections of the even mode that may occur, as well as the non 50 Ω reference impedance for inter-stage matching, special care must be taken for ensuring stability and a method based on the Nyquist stability criterion [12] has been used in order to perform accurate linear stability analysis.

The circuit first is split so as to unfold three planes A, B and C (figure 2), and then stability analysis is performed respectively considering even and odd mode response. Local stability is assumed if the product of refection coefficient $\Gamma_g \cdot \Gamma_e$ locus does not exhibit any clockwise encirclement of the point 1+j·0 for both even and odd mode circuits. Nyquist loci plots of the three planes A, B and C (figure 7), indicate stable circuit operation. Impulse response of the active balun further confirms this stability (figure 8).

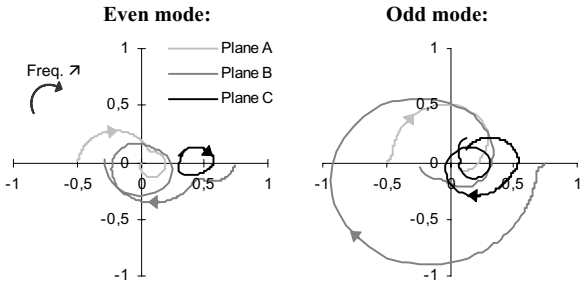

Fig. 7. Nyquist loop for Even and odd modes at A, B and C loci (see circuit schematic on figure 2).

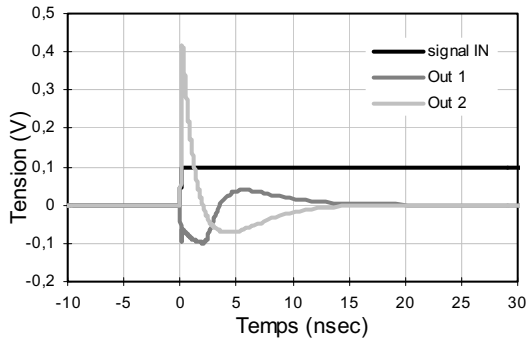

Fig. 8. Transient analysis of the active balun confirms stable operations.

VII. CONCLUSION

An improved active two stage differential power splitter has been demonstrated. It involves two CE and CC cascaded differential pairs featuring dedicated impedances for connecting each of the common node to ground. It significantly improves the balanced performance in the high microwave frequency range with respect to the conventional technique that uses a common node impedance as large as possible.

These dedicated impedances are a capacitor for the first common emitter stage and an inductor for the second common collector one. The overall circuit has been laid out with a special care on its symmetry and interconnections. As a result, a CMRR near 43 dB in the 20 GHz frequency range, i.e. a maximum 0.35° phase and 0.12 dB amplitude unbalance are anticipated. It also features broadband operations in the 6-27 GHz frequency range over which a CMRR value better than 29 dB is achieved. The circuit processing is near from completion and measured results will be available very soon.

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REFERENCES

[1] Yeong J. Yoon & al. "Design and Characterization of Multilayer Spiral Transmission-Line Baluns" IEEE Trans. on MTT, vol 47, n°9, Sept. 1999

[2] Dickson T.S. Cheung, J.R. Long, R.A. Hadaway & D.L. Harame "Monolithic Transformers for Silicon RFIC Design" IEEE BCTM 1998

[3] M. C. Tsai & al. "A Compact Wideband Balanced Mixer" IEEE MTT-S Digest, 1994

[4] A. H. Baree & I. D. Robertson "Analysis and Design of Multi-Octave MMIC Active Baluns Using a Distributed Amplifier Gate Line Termination Technique" IEEE MTT-S Digest, 1995

[5] Huainan Ma, Sher Jiun Fang, Fujiang Lin, Hiroshi Nakamura "Novel Active Differential Phase Splitters in RFIC for Wireless Applications" IEEE Trans. on MTT, vol 46, n°12, Dec. 1998

[6] F. Van Raay, G. Kompa "Design and Stability Test of a 2-40 GHz Frequency Doubler with Active Balun" IEEE MTT-S Digest, 2000

[7] J. Lin & al. " silicon MMIC active balun/buffer amplifier with high linearity and low residual phase noise" IEEE MTT-S Digest, 2000

[8] F. Temcamani, B. Delacressonniere, P. Lida, J.L. Gautier "Limitations of the even mode rejection in differential structures" 23rd European Microwave Conference, 1993

[9] C. Viallon, T. Parra "Improved Differential Structures for Balanced Microwave Applications" Submitted to IEEE Asia Pacific Microwave Conference, 2003

[10] D.E. Bockelman, W.R. Eisenstadt "Combined Differential and Common-Mode Scattering Parameters: Theory and Simulation" IEEE Trans. on MTT, vol 43, n°7, July 1995

[11] D.E. Bockelman, W.R. Eisenstadt "Combined Differential and Common-Mode Analysis of Power Splitters and Combiners" IEEE Trans. on MTT, vol 43, n°11, Nov. 1995

[12] M. Odyniec "Stability criteria via S-parameters" 25th European Microwave Conferences, 1995