Multifunction MMIC For Miniaturized Solid State Switch Matrix

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Abstract **- This paper describes a new multifunction MMIC expressly designed for a reconfiguration matrix equipment. This MMIC has been developed using a standard PHEMT process and includes two switches, a totally switchable-off amplifier and a temperature compensation circuit. The complete circuit has also been designed to interface a standard CMOS control level. Performed simulations and obtained results demonstrate the effectiveness of this approach in reaching compactness and reliability of satellite equipment.**

I. Introduction.

Due to the well known consequent benefits in satellite telecommunication equipment, one of the most challenging effort in MMIC design, is represented by the capability to include more functions on the same chip[1]. The aim of multifunction approach is not only the reduction of connections at equipment level but also the consequent improvement in terms of repeatability and production yield. Equipment like reconfiguration matrix include several passive and active devices cross connected to create the proper RF path where is requested and therefore represent one of the best example in which the multifunction MMIC approach can be effectively used. The possibility to include switching and amplification functions within a single MMIC is, quite attractive since the equipment can be made very compact keeping at the same time isolation and insertion loss performances [2].

This paper describes a new multifunction MMIC that has been expressly developed for this kind of applications. It includes two switches, a switchable-off amplifier and a temperature compensation circuit in a relatively small area using a standard 0.25 um PHEMT process. MMIC has been also designed to be compatible with a CMOS Control Voltage and standard 5 Volts bias level. Performed simulations and obtained results demonstrate the effectiveness of this approach.

II. Overview Of Reconfiguration Matrix.

Developed MMIC have to be used in a switch matrix in which 8 input ports can be simultaneously connected to any of the 8 output ports without blocking any other interconnection. As shown in figure 1, the whole equipment is composed of a microwave section, a control section and a DC/DC converter. Each section has a prime and a redundant circuitry.

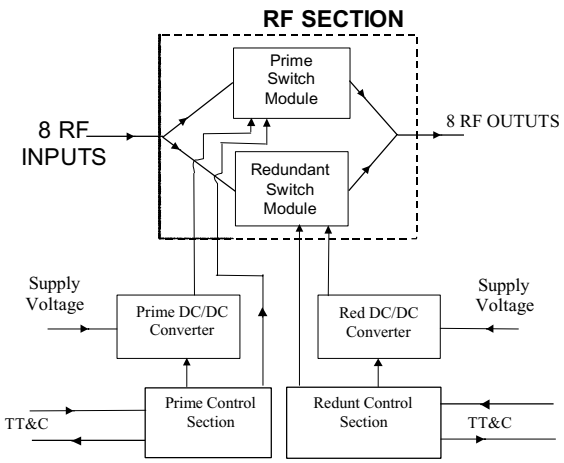

Figure 1. Reconfiguration Matrix.

Figure 2 shows a comparison between two possible approach for the microwave section:

In the conventional approach the input section includes all passive slpitters, a bench of Voltage Variable Attenuators, and a bench of switches. The cross section allows each of the eight RF input signals to be interconnected to each one of the output ports.

The out put section includes a bench of switches, a power combiner and a bench of Medium Power Amplifier.

In our approach the developed multifunction MMIC allows a very simple and compact housing.. Switching and amplification functions can be included in a single and very compact section. In the "ON" state the cross matrix is required to have a minimum gain between the connected RF paths while the isolation between all the not connected paths must be minimum 50 dB. Another important requirement for this equipment is to have low power consumption when the RF path is not active. Furthermore a good VSWR in both states is also required. Requirements at equipment level have been traduced in specifications at MMIC level reported in table I.

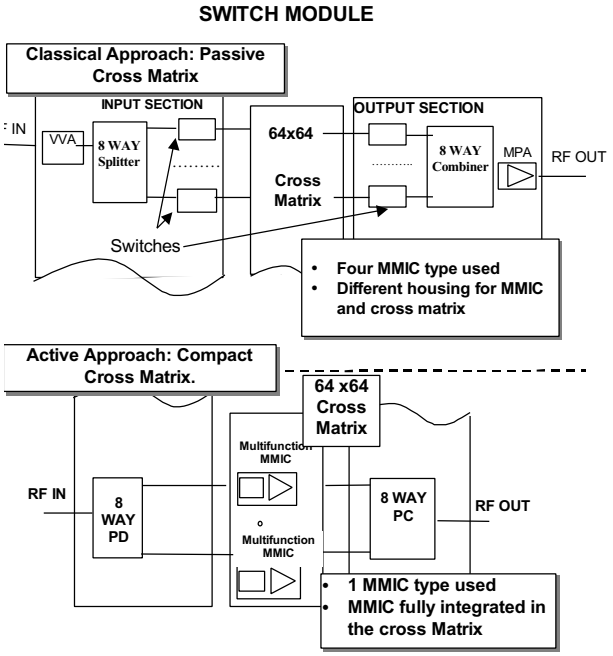

Figure 2. Comparison between conventional and multifunction MMIC approach.

PARAMETER	VALUE	UNIT
Small Signal Gain	23	dB
1 dB C.P.	14	dBm
Gain Flatness	1	dBpp
Insertion loss in off conditions	30	dB
Input / Output Matching (S11, S22)	-13	dB
Supply Voltage	5	V
Switching Voltage	0 ÷ 5	V

TABLE I. MMIC Specifications.

III. MMIC DESCRIPTION.

Block schematic of the developed MMIC is shown in figure 3. As per requirements at equipment level, main features of this circuit are:

- MMIC has to be totally switched off when the isolation state is required.
- Good matching conditions at input and output ports are necessary in isolation and low insertion loss state.

The MMIC structure has three sections: Input/output switches, True Amplifier, CMOS interface with temperature compensation circuit. Each section will be separately described.

A. Input / Output Switches.

Input and output switches are SP2T type; each switch is composed of two cold FETs in series configuration. One branch is terminated on a 50 ohm resistor through a λ/4 Microstrip Line, while the other branch is terminated directly on the Amplifier Input.

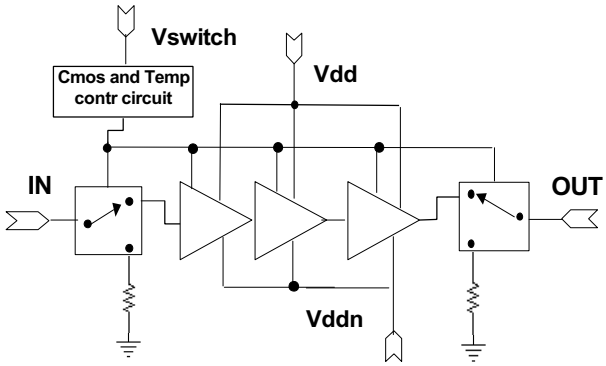

Figure 3. Block schematic of developed Multifunction MMIC.

When Vsw is low (0 Volts) the FETs are in low impedance status and Isolation is minimum. When Vsw is high (5 Volts) both FETs are in high impedance condition and the isolation is maximum. λ/4 transformer allows to have good matching in both conditions. Switch schematic is shown in figure 4.

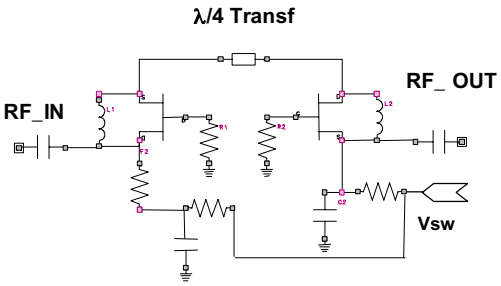

Figure 4. Switch schematic.

B. Amplifier section.

A three stages approach has been used for the Amplifier section. The three stages are dimensioned to have the required gain and output power performances at the same time. Each stage requires separate drain and gate biasing. Proper Drain voltage for each stage is obtained from a common Vdd trough separate resistors while separate gate voltage is obtained from a common interface designed to have at the same time shift level and complementary voltages generators for CMOS compatibility and voltage swing necessary for temperature compensation.

C. CMOS and temperature compensation interface.

This interface has been conceived as biasing and compensation circuit that allows to pinch off both switches and amplifier FETs. Switches have been designed to be switched with a single voltage, so this interface uses a level shifting to proper adjust the

available external CMOS level to the gate voltage required for switching function. Gain compensation vs temperature is based on concept already proposed in literature using diodes [3], and extended in this work, to FETs. Compensation is not applied on the switches, since for Cold FETs variations vs temperature has been estimated very low compared to the active part of the MMIC. The temperature compensation circuit acts on Ids variation vs temperature. When the temperature changes, I_{ds} and gain variation of each amplifier stage are compensated by a properly dimensioned and controlled variation of gate polarization. Figure 5 shows a simple schematic of the implemented circuit.

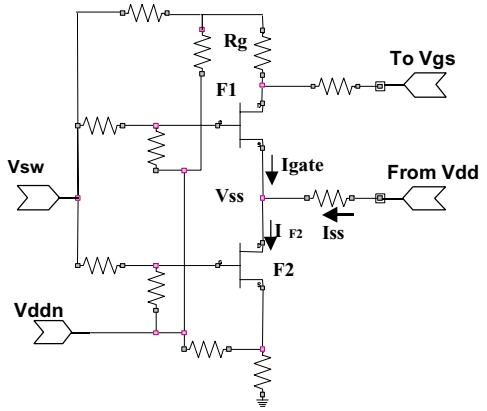

Figure 5. Simple Schematic of Temperature Compensation Circuit.

Two important issues related to space applications have been taken into account in the design of the compensation circuit: the limitation of the active devices Junction Temperature to 110 °C and the power consumption. Both these issues limit the effectiveness of the compensation and the double FET structure biased with high value resistors allows to have the best tradeoff between maximum compensation and system requirements.

D. MMIC Operation.

To keep the compatibility with CMOS Level for the control Voltage, and have the right dynamic, this MMIC requires both negative and positive fixed voltages while the switching control voltage (Vsw) switches the circuit from high to low isolation state. The MMIC can actually operate in three different conditions: keeping fixed Positive and Negative voltages it is possible to reach required nominal isolation condition just acting on Vsw. When also the positive and negative voltages are switched off, the MMIC is put in a maximum isolation condition. The ON condition is obtained with Vdd= 5V.; Vddn = -5V. and Vsw=0. The OFF condition is obtained with: Vdd =5V.; Vddn = -5V. and Vsw = 5V. In this case the control circuit brings all the active FETs in Pinched-off condition: 20 dB isolation between input and output are reached with very small power consumption. When Vdd= 0V.; Vddn = 0V. and Vsw =5V. it is possible to get the maximum isolation between input and output with no power consumption.

IV. Tecnology Description.

Presented MMIC was developed in a multi-project run using a standard 0.25 um Power PHEMT process. Chosen foundry was UMS and typical process parameters are: Ft = 50 GHz , Ids typical of 500mA/mm, Pinch-off Voltage of 0.9 V, Breakdown Voltage=12 V and Transconductance=300 mS/mm. The chosen process is already space qualified and it has already been used for other satellite applications and a total of 2 wafers were processed.

V. Simulations And Measurements.

Simulations have been performed using both LIBRA® and ADS® with UMS design kit. To properly simulate the temperature behaviour of active elements, linear and non linear models, have been extracted from several measurements performed on single FET and representative reference amplifiers expressly tested for this purpose. Bonding wires effect has been inserted in the simulation to limit the influence of parasitic effects due to final housing. Finally, to verify the effectiveness of the compensation circuits a simulation has been performed comparing the amplifier with and without compensation circuit. Simulations are reported in figures 6, 7, and 8. Figure 9 shows measurements performed on fixture. Fixture losses are in the range of 1.5 dB, so measured gain resulted a little higher than expected. Precautions on biasing have been taken to avoid unwanted oscillations. As can be seen a total relative isolation of 78 dB has been measured. Input and output return loss resulted in the range of 10 dB at both gain or isolation status. Performance vs temperature variation is reported in figure 10. Compensation is quite good and comparable with simulations.

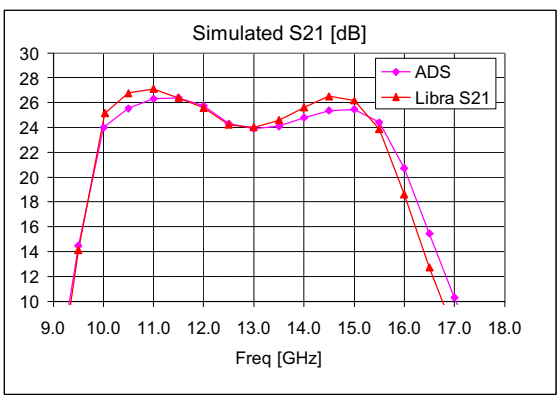

Figure 6. Simulation at maximum gain condition.

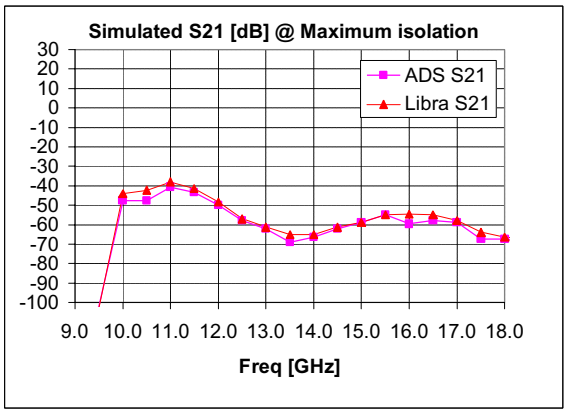

Figure 7. Simulation at minimum gain condition.

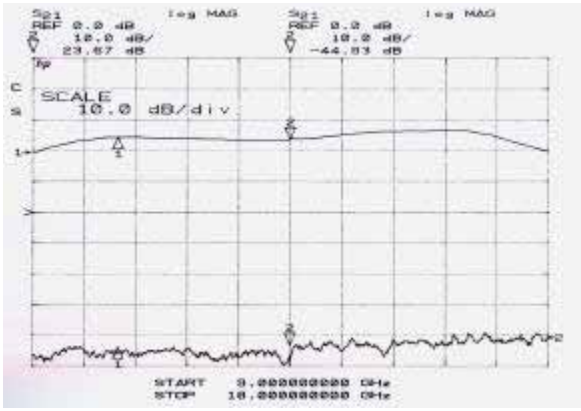

Figure 9. Measured Gain and Isolation performances.

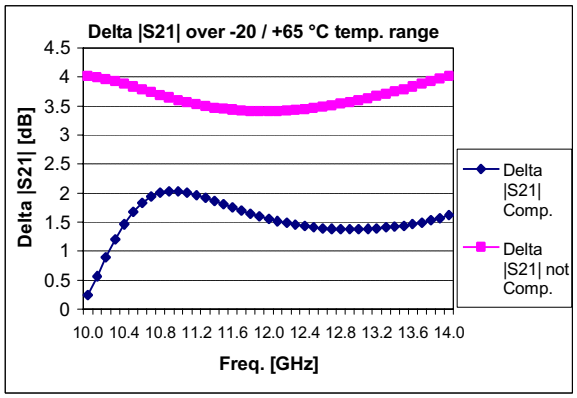

Figure 8. Simulated comparison between compensated and uncompensated behavior the same amplifier.

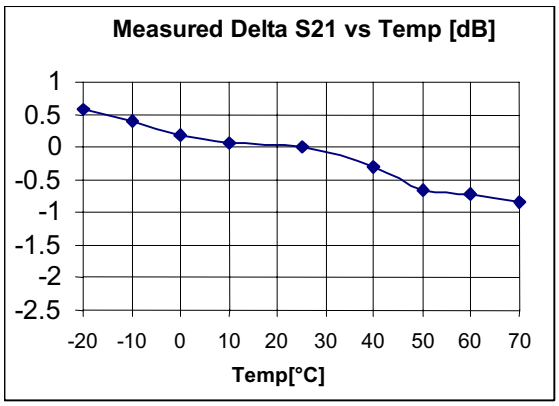

Figure 10. Measured delta gain versus temperature variation.

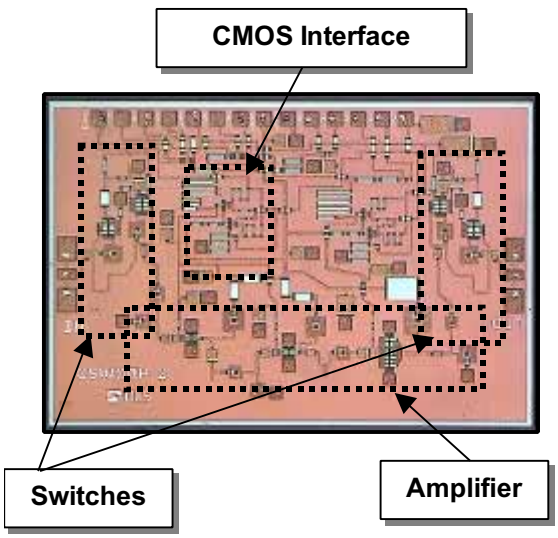

Figure 11. Realized MMIC. Total dimensions are 3x2 mm.

VI. Conclusions.

A new Multifunction MMIC has been developed to help size reduction in reconfiguration switch matrix. This paper demonstrates that GaAs technology is already assessed to design and develop multifunction MMIC with a good success. Obtained results are encouraging and can be the basis for further development of truly competitive equipment.

Aknowledgements.

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[3] K. Yamauchi et al.; X Band MMIC Power Amplifier with On chip Temperature Compensation circuit; *2001 IEEE MTT-S Digest.*