Materials to Microsystems: Heterogeneous Integration Technologies

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***ABSTRACT* — Microsystems technology is increasingly comprised of multi-function devices and materials. Heterogeneous integration technologies are being developed to enable the flexible integration of high-performance devices, materials, and circuits. In our approach, the processing required for integration, such as substrate removal and bonding, is coupled with pre- and post- processing to enable new device and materials configurations not achieved in standard fabrication sequences. Materials and device processes and designs must be considered differently in the context of integration. Herein, we examine these issues specifically for InAs-, InP- and GaN- based heterojunction electronic and optoelectronic device integration processes.**

I. Introduction

For a number of decades, devices and materials research has been focused on the goal of integrating dissimilar technologies to achieved multi-functionality in a compact, economical chip form. Materials research has lead the way- from direct growth of compound semiconductors on silicon to engineering to the formation and exploitation of "compliant" substrates [1] to control defects in active layers. Direct heteroepitaxy continues today as an active and viable approach for some materials systems. Recently, however, more emphasis has been placed on advanced combined materials and device fabrication that combine packaging and integration from the wafer-scale to the device-scale. While a range of challenges- from circuit design to bonding technology to modified materials growth approaches - must be addressed to enable heterogeneous integration; enhanced flexibility in microsystem design is also enabled. Active packaging (1), a term first used in 1994 [2], describes such a generalized approach to concurrent package and device design. Our use of the term focuses on the notion that the processing required for integration, such as substrate removal and bonding, is coupled with pre- and post-processing to enable new device configurations not achieved in a standard growth, fabrication, and packaging sequence. An active packaging approach enables collector-up HBTs, and inverted metal-semiconductor-metal devices with enhanced responsivity and alignment tolerance.

Our previous and current research focuses on the integration of a range of materials and devices, such as InP-based heterojunction devices, GaN metal-semiconductor-metal detectors, and InP-based detectors with Si CMOS electronics or on Si wafers. We are also investigating the use of bonded substrates for regrowth, such as strained layers on InGaAs substrates. Examples of these technologies are discussed in below.

II. Integration of InP-based Heterojunction Bipolar Transistors

The process for the integration of InP-based materials, such as AlInAs-GaInAs or InP-GaInAs HBTs, is that of selective etching and wafer-scale direct and low temperature bonding. The HBT layer to be bonded is grown in an inverted fashion (collector-up) so that upon bonding and substrate removal standard emitter-up fabrication processes can be exploited. Key materials issues must be considered during both epitaxy and the bonding process. One of these is the modification of HBT material properties as a consequence of the required inverted growth process. Be diffusion from the base to the emitter is a common issue to be controlled during HBT growth. With inverted growth, this problem is mitigated as the key interface is now grown emitter first, and dopant segregation effects are thus less important. The lattice-match of the HBT layer structure to the InP substrate is critical, and the initial oxide removal process (wherein As exchanges with P during oxide removal) can introduce defects which thread into the subsequent layer. We have found that these processes are very important to integration - dislocations that thread into the layer can be sites for enhanced etching during substrate removal, and can lower device fabrication yield. Post-bonding strain or warpage is also critical. A low temperature (or room temperature) bonding process is used so that coefficient of thermal expansion (CTE) mismatches between the device epitaxial layers and the handle wafers (such as GaAs or Si) are minimized. The bonding process was developed at the University of Wisconsin. Bonding must yield an interfacial energy high enough to enable subsequent mechanical processing.

The specific process is as follows: the substrate surfaces are exposed to an oxygen plasma and then rinsed and placed in direct contact with flags positioned at the wafer periphery. Contact begins at the center. For InP bonding the substrate is removed after bonding via selective etching using an HCl/H_2O etch [reference].

A full 2"-wafer low-temperature bond and transfer has been applied to GaInAs-AlInAs HBTs to integrate devices onto a GaAs platform. Ultimately, other substrates, such as sapphire or silicon will be used for the

package. 50x50 μm^2 devices show only small changes in relevant properties – breakdown and turn-on voltages, leakage currents, and ideality factors. Fig. 1 shows a comparison of emitter-base I-V characteristics of the as-grown structure (R17) and the bonded structure (R178). In this particular case, the leakage current is, in fact lower, for the bonded HBT structure [3].

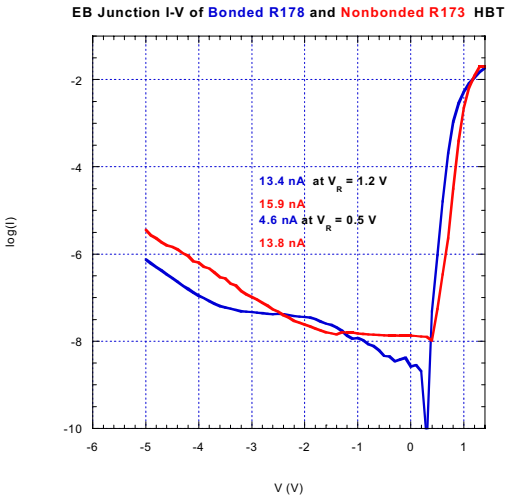

Fig. 1. IV Characteristics of HBT (Bonded and Reference)

In addition to the bonding of lattice-matched device wafers, we are also exploring the limits to bonding of strained layers for subsequent processing, including regrowth on novel ternary substrates. An example would be the preparation of an InGaAs on GaAs (or some other handle wafer) substrate for device regrowth. We have achieved successful bonding of InGaAs to GaAs (with a lattice mismatch of about 3.8%) and verified that the bonded layer is defect free after thermal excursions. This success in InGaAs/GaAs wafer bonding opens up vast opportunities for novel device integrations. The wafer bonding is carried out at room temperature followed by a thermal anneal. TEM bright-field images show that the 0.41-μm-thick InGaAs layer bonded to a GaAs wafer substrate is free of any dislocations or other extended defects. The InGaAs surface is atomically flat, suitable for subsequent growth of epitaxial layers and device fabrication.

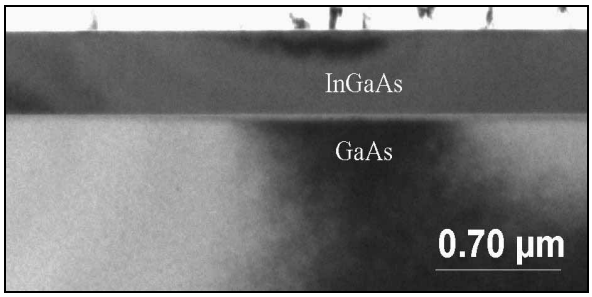

Fig. 2. Strained InGaAs bonded to GaAs (TEM: T.S. Kuan)

III. INTEGRATION OF PHOTODETECTORS WITH SI

Metal-semiconductor-metal (MSM) photodetectors are important for a range of optoelectronic interface applications. We have integrated both GaN and InGaAs photodetectors onto Si substrates and circuits in various formats, including directly on wafer (within a specially designed chip) or embedded in a polymer waveguide. Bonding an inverted MSM onto a metal pad in a Si circuit improves device performance: the photodetector responsivity is improved by the placing the metal contact fingers beneath the active area (thus eliminating finger shadowing), yet the I-MSM retains the small capacitance per unit area advantage compared to pin devices. We have recently shown excellent thin film device performance enabled using this active packaging approach. These InGaAs-based thin film I-MSM detectors had a measured dark current 0f 1.91 nA and a responsivity of 0.16 A/W at 5V at λ=1.32μm. High speed characterization of the I-MSMs was performed using an electro-optic sampling system with the thin film MSM integrated onto a coplanar transmission line. The measured impulse response using the electro-optic sampling system showed a 6.3 ps FWHM. These PDs, which are 40 μm in diameter, are very large in area compared to other reported PDs which operate at a FWHM of less than 10 ps. [4] To our knowledge, this device is the fastest vertically illuminanated PD with such a large detection area. Recently, we have developed and exploited an embedded inverted MSM process to embed these thin film detectors directly into waveguide structures, as shown in Fig. 3. This process begin with placing the inverted MSM on a metal contact on an arbitrary host substrate (high temperature FR-4, silicon, glass, and ceramic include the substrates that have been integrated with thin film I-MSMs embedded in waveguides). The waveguide cladding materials, such as BCB, is spin-coated onto the substrate surface and then planarized with a CMP process. The waveguide core material, Ultem, is then spin-coated, and finally the waveguide channel is patterned with a dry etch. Fig. 3 shows an image of an I-MSM embedded into a polymer waveguide. Such configurations enable fully functional active planar photonic circuits without beam turning for photon emission and detection..

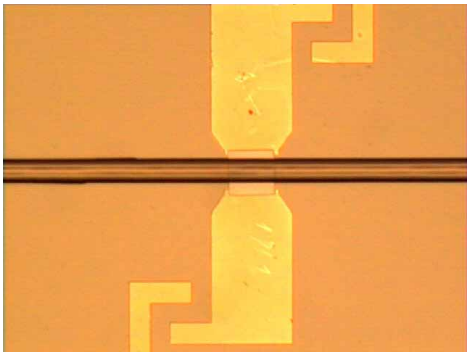

Fig. 3. I-MSM photodetector embedded in a BCB polymer waveguide

The integration of GaN materials and devices is particularly challenging. Substrate removal and etching made more difficult given that the most commonly used substrates- sapphire and SiC- are particularly difficult to etch. However, GaN offers unique microsystems functionality including advanced signal processing for integrated UV optical imaging arrays, and advanced packaging and automated tuning for high-power electronic devices. We have developed an approach for achieving device-quality GaN epitaxial material by Molecular Beam Epitaxy (MBE) concurrent with an integration process, by exploiting the alternative lithium gallate ($LiGaO_2$ or LGO) substrate. As described below, these substrates offer some specific advantages over the more commonly substrates. In the integration context, we can exploit a selective wet chemical etch and device- and circuit-scale bonding process.

IV. GROWTH OF GAN ON LGO FOR HETEROGENEOUS INTEGRATION

The growth of GaN epitaxial layers on LGO offers distinct advantages in achieving device quality material. Hexagonal GaN has a lattice mismatch of only –0.19% to the b-axis of LGO [5]. The dislocation density of GaN grown directly on LGO is estimated to be in the $10^7 – 10^8$ cm^{-2} [5,6], compared to $10^8–10^{11}$ cm^{-2} for direct heteroepitaxial growth of GaN on sapphire and SiC. The electronic and structural characteristics of AlGaN - GaN heterojunctions are inferred from the conductivity of two-dimensional electron gases (2DEG) induced at the interface. We have achieved 2DEG mobilities of > 1300 cm^2/Vs at 300K with a sheet charge was 7.7 x 10^{12} cm^{-2} [7]. The structure was grown directly on LGO with a 0.8 µm GaN buffer followed by 35 nm of AlGaN.

We have demonstrated MSM photodetectors grown on LGO for integration with Si. Unintentionally-doped GaN was grown on (001) LGO was grown using plasma-assisted radio-frequency molecular beam epitaxy. A five-period $Al_{0.4}Ga_{0.6}N$/GaN superlattice was deposited as part of the nucleation layer, followed by a 1-µm thick unintentionally doped GaN epitaxial layer. Devices were fabricated and tested before and after integration on a SiO_2/Si wafer. Interdigitated-finger MSM devices were 47 µm long, with 2 µm finger width and 5 µm finger spacing, and a detection area of 50x50 μm^2. The Schottky contacts were 500Å Pt/2000Å Au, deposited using electron beam evaporation. A cleaning step used to remove the oxide on the GaN surface consisting of a hydrofluoric (HF) acid dip for 1 min and warm ammonium hydroxide (NH_4OH) for 15 min prior to the metallization lowered the MSM dark current by several orders of magnitude.

The integration process follows the typical process for InGaAs on Si but with some material specific changes required for GaN. Mesas were patterned on the GaN surface using a photoresist mask and dry etching in a PlasmaTherm inductively coupled plasma (ICP) system using Cl_2/BCl_3/Ar gases with flow rates of 8 sccm/12 sccm/5 sccm operating at a 500 W plasma power, 90 V DC bias, and a substrate holder temperature of 15 ^oC. Under these conditions, the etch rate of GaN ranged from 2000 Å– 2400 Å per minute while the etch rate of the substrate was <10 Å/min. Thus, the etch stops at the GaN/substrate interface. The GaN mesas were then coated in Apiezon W to protect and support the GaN mesas during the subsequent substrate removal process.

The GaN epitaxial layer is impervious in terms of practical etch rate to most wet chemical acid solutions, thus, removal of the substrate from the GaN epitaxial layer is highly selective. The sample was kept in $HF:H_2O$ (1:10) for approximately two hours to remove the $LiGaO_2$ substrate. The etch rate of the substrate in $HF:H_2O$ (1:10) is approximately 4.5µm/min. The mesas embedded in the Apiezon W were bonded to SiO_2 (9000Å) coated Si substrate through contact bonding. The Apiezon W is then dissolved with trichloroethylene, leaving the devices bonded to the SiO_2/Si host substrate. Fig. 4 shows an SEM micrograph of a 170 µm x 90 µm mesa, 1 µm thick GaN thin film MSM photodetector bonded to a SiO_2/Si substrate [8-10].

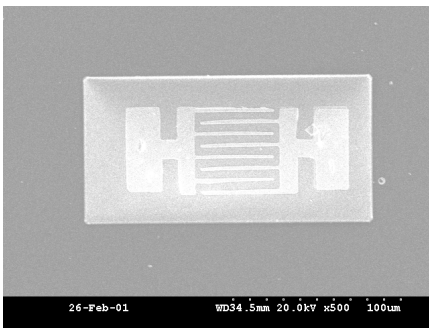

Fig. 4. GaN thin film MSM detector bonded onto a SiO_2/Si host substrate.

This process is a low temperature process which predicts the successful implementation of this process for integration with Si CMOS circuitry. The most successful competing process is that of Wong, et al. They have reported a process to separate GaN-based devices using a

laser separation technique that decomposes the interface between the GaN and the sapphire substrate [11,12].

The dark current and photoresponse of the GaN MSMs before and after bonding were compared.The measured dark currents and responsivities for the on-wafer MSMs and the thin film MSMs after bonding to the SiO_2/Si host substrate are excellent and show the efficacy of this process. The dark currents of 0.577 pA at 5V and 11.46 pA at 50V on-wafer degrade slightly to 0.627 pA at 5V and 13.36 pA at 50V after bonding.

A key issue in the integration of GaN (on LGO) with Si (or other samples) is the as-grown strain in the GaN after the growth process. We have observed some yield problems due to the built-in and anisotropic strain. We have recently characterized the strain in the GaN and found that it results primarly from the CTE mismatches in the GaN and LGO, not in the lattice mismatch. Thus, we are investigating the use of built in strain compensation in buffer layers.

V. Conclusion

Integration technologies are critical to advanced microsystem design. Our approaches have spanned the range from wafer-scale low temperature bonding to device-to-circuit scale engineered devices. In order to achieve excellent microsystem performance, materials to device design must be viewed in the context of integration.

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