# Integrated Circuits Based on 300 GHz $f_T$ Metamorphic HEMT Technology for Millimeter-Wave and Mixed-Signal Applications

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*ABSTRACT* — **Advanced circuits based on metamorphic HEMT (MHEMT) technologies on 4" GaAs substrates for both millimeter-wave, and mixed-signal applications are presented. Extrinsic cut-off frequencies of $f_t$ = 293 GHz and $f_{max}$ = 337 GHz were achieved for a 70 nm gate length metamorphic HEMT technology. The MMIC process obtains high yield on transistor and circuit level. Single-stage low-noise amplifiers demonstrate a small signal gain of 13 dB and a noise figure of 2.8 dB at 94 GHz. An amplifier MMIC developed for D-Band operation features a gain of 15 dB at 160 GHz.The achieved results are comparable to state-of-the-art InP-based HEMT technologies. In order to realize 80 Gbit/s digital circuits, a process with 100 nm gate length enhancement type HEMTs with a transit frequency of 200 GHz is used. Three metalization layers are available for interconnects. The parasitic capacitance of the interconnects is kept low by using BCB and plated air bridge technology. Based on this process, static and dynamic frequency dividers achieve a maximum toggle frequency of 70 GHz and 108 GHz, respectively.**

## I. Introduction

In recent years there has been an increasing interest in high frequency devices for operation up to 100 GHz, and beyond. Typical applications for these devices are low-noise or power ICs for radar and sensor systems, and digital ICs for fiber optic communication up to 100 Gbit/s. Generally, there are three competing technologies in this field, namely SiGe HBTs, III/V HBTs, and III/V HEMTs. However, the latter combines the potential for both ultra low noise, and high power operation at millimetre-wave frequencies.

Therefore, InAlAs/InGaAs based High Electron Mobility Transistors (HEMTs) have been used successfully to realize circuits in the upper frequency bands [1]. The transit frequency of the single transistor can be improved by increasing the indium content in the channel and/or reducing the gate length. Advantages of a metamorphic technology using GaAs instead of InP as substrate include the larger substrate size resulting in reduced chip costs, better mechanical stability, and better availability of GaAs substrates up to 6'' compared to InP. This paper reports on state-of-the-art depletion and enhancement type metamorphic HEMT (MHEMT) technologies, and related circuit applications.

For mixed-signal circuits, enhancement type HEMTs (E-HEMTs) allow more compact design layouts compared to depletion type HEMTs (D-HEMTs).

## II. Technology

The D-HEMTs are grown on 4" semi-insulating GaAs wafers by molecular beam epitaxy (MBE). A linear graded metamorphic $In_xAl_{0.48}Ga_{0.52-x}As$ (x = 0 → 0.52) buffer is grown on the substrate to adapt the lattice constant. The active channel layer is divided in two $In_xGa_{1-x}As$ layers with x = 53 % and x = 80 % In concentrations. This composite channel is used to reduce the electron-hole pair generation caused by hot electrons.

The E-HEMT features an MBE structure with a linear graded quaternary AlInGaAs buffer to relax the lattice constant. A single sided $6.0 \times 10^{12}$ $cm^{-2}$ doped composite channel with 53 % and 65 % In is used. The 10 nm InAlAs barrier layer is capped with a 17 nm InGaAs $6.0 \times 10^{18}$ $cm^{-3}$ Si-doped layer.

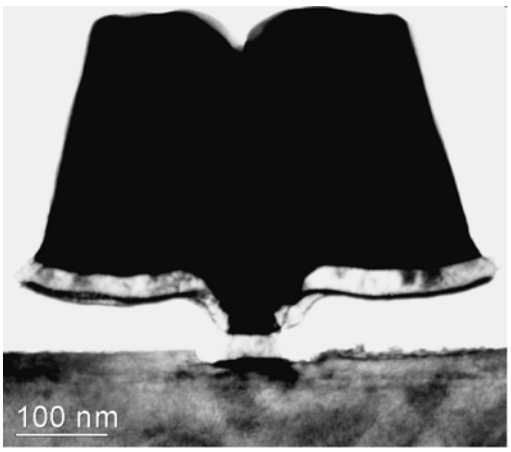


*Fig. 1. TEM cross section of a 70 nm gate.*

The transistor mesa is wet chemically etched and NiGeAu is deposited for the ohmic contacts. Gate definition is performed using electron beam lithography in a three layer resist (PMMA) process, and wet chemical recess etching. A Pt-Ti-Pt-Au layer sequence

is used for the gate metalization. A T-gate with large gate cross section is developed for reducing the gate resistance and improving the device noise figure (Fig. 1).

The process further includes CVD deposited SiN passivation, NiCr thin film resistors, MIM capacitors and two-layer metalization including a 2.7 µm thick plated Au layer air bridge technology.

The process for the mixed-signal ICs features an additional evaporated Au based interconnect layer, and a 1.2 µm BCB (benzocyclobutene) dielectric layer between the first and the second metal layer allowing low parasitic capacitance of the interconnects. The vias through the BCB layer with a minimum diameter of 1 µm are defined by dry etching.

## III. Device Performance

The output characteristics of the D-MHEMT are shown in Fig. 2. The $R_{on}$ is 0.5 Ωmm. The on-state breakdown voltage $V_{BD,ON}$ of 1.7 V is measured for a gate current of 1 mA/mm.

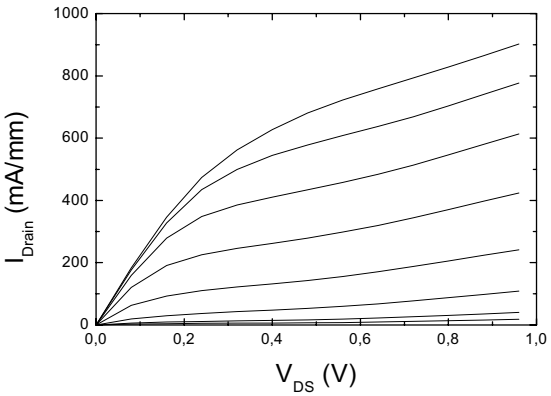


*Fig. 2. I/V- characteristics of the 70 nm MHEMT.*

The yield at device level is higher than 90 % for a gate width of 120 µm (Fig. 3). Extrinsic cut-off frequencies of $f_t$ = 293 GHz and $f_{max}$ = 337 GHz were achieved for a 2 x 30 µm device, as shown in Fig. 4. Average values of 290 GHz for $f_t$ and 1450 mS/mm for the transconductance were obtained.

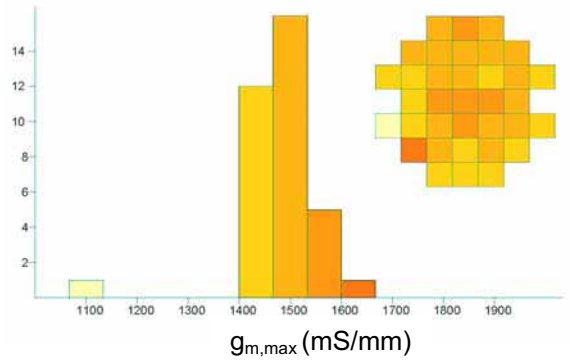


*Fig. 3. Topogram of the maximum transconductunce $g_{m,max}$ across a 4" wafer for a 2 x 60 µm device.*

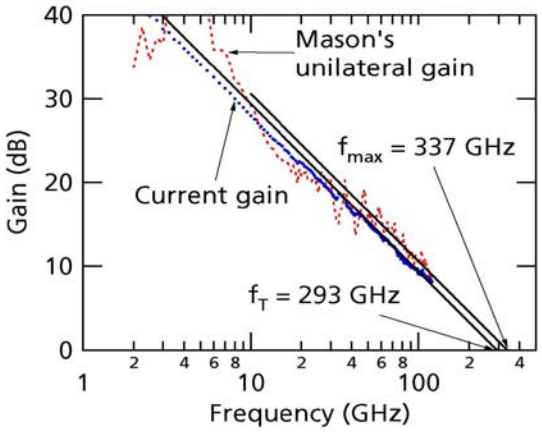


*Fig. 4. Figures of merit $f_t$ and $f_{max}$ for a 2 x 30 µm D-HEMT device.*

For the E-HEMT process, source resistances below 0.25 Ωmm with a variation of 0.03 Ωmm across the 4" wafer are achieved, the contact resistance of the ohmic contacts is less than 0.1 Ωmm. A maximum transconductance of 1500 mS/mm and a threshold voltage of $V_{th}$=+150 mV (linear extrapolation of $\sqrt{I_D}$ ) is achieved. The high transconductance is needed to speed up the inverter stages designed in source coupled FET logic whereas the positive threshold voltage simplifies the shifting of the bias level between the stages. $f_t$ and $f_{max}$ values of 200 GHz for a 2 x 60 µm device are obtained. The variation of the threshold voltage across 4" wafers is less than 50 mV. The on-state breakdown voltage of the devices is 2.5 V. The device performance of our metamorphic enhancement type HEMTs is comparable to state-of-the-art InP based 100 nm E-HEMTs.

An important issue is the reliability of MHEMTs because of the high dislocation density in the metamorphic buffer. To achieve superior life times in an air environment, a 270 nm thick two-layer SiN passivation is used.

In order to determine the lifetime, accelerated reliability tests were performed in air at 200 °C, 225 °C and 235 °C channel temperature, and $V_{DS}$=1 V. A lot of eight devices is used for each temperature. Based on a 10 %-$g_{m,max}$ degradation failure criterion and the log-normal distribution, an activation energy of 1.3 eV and a median life time of $1x10^6$ h at 125 °C was determined for the 70 nm D-HEMT, and an activation energy of 1.5 eV and a median life time of $1.1x10^6$ h at 125 °C for the 100 nm E-MHEMT device. The activation energy for the 70 nm D-HEMT is significantly smaller than the activation energy of 1.8 eV obtained for the related 100 nm D-HEMT technology with 65 % instead of 80 % In in the channel [2]. The higher electric field in the 70 nm transistors and the higher saturation velocity of the 80 % In-channel increases the electron temperature and thus reduces the activation energy of the degradation mechanism. The achieved lifetime is comparable to InP-based HEMT processes [3], and no negative influence of the metamorphic buffer has been observed so far.

| | D-HEMT 70 nm | E-HEMT 100 nm |
|---|---|---|
| $R_C$ | <0.1 Ωmm | <0.1 Ωmm |
| $R_S$ | 0.2 Ωmm | 0.25 Ωmm |
| $I_{D\,max}$ | 850 mA/mm | 650 mA/mm |
| $V_{th}$ | -250 mV | +150 mV |
| $V_{DB,on}$ | 1.7 V | 2.5 V |
| $g_{m,max}$ | 1450 mS/mm | 1500 mS/mm |
| $f_t$ | 290 GHz | 200 GHz |
| $f_{max}$ | 330 GHz | 200 GHz |

TABLE I: AVERAGE ELECTRICAL DC AND RF PARAMETERS OF THE MHEMT PROCESSES

The measured transistor parameters for both processes are listed in Table 1.

## IV. CIRCUIT RESULTS

For active and passive millimetre-wave imaging applications requiring very low noise figures and broadband gain characteristics, a 94 GHz low-noise amplifier (LNA) MMIC was developed [4]. The amplifier circuit is optimised to achieve high gain in combination with a very low noise figure. Therefore a cascode configuration consisting of a series connection of one HEMT in common source and one in common gate configuration is utilized which exhibits a maximum stable gain of 22 dB at 94 GHz, as illustrated in Fig. 5.

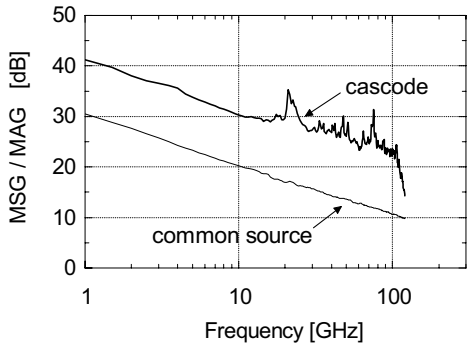


***Fig. 5.*** *Measured MSG/MAG of an un-stabilized 2 x 30 µm cascode MHEMT and a 2 x 30 µm common source MHEMT.*

Fig. 6 shows a photograph of the fabricated 94 GHz low-noise amplifier MMIC. A very small chip-size of 1 x 1 mm$^2$ could be realized. The gate width of the cascode FETs is 2 x 30 µm. The amplifier circuit demonstrated a small signal gain of more than 12 dB between 75 and 100 GHz as illustrated in Fig. 7. The on-wafer measured noise figure is 2.8 dB between 80 and 95 GHz. This compares favourably with previous LNA results based on metamorphic HEMT technology [5] and is in accordance with the best noise figures published for InP based HEMTs [1]. Typical supply voltages were 0.15 V at the gate, 0.8 V at the second gate, and 1.6 V at the drain. The measured amplifier gain at 94 GHz over all 35 circuits shown in Fig. 8 demonstrates the high process yield and uniformity.

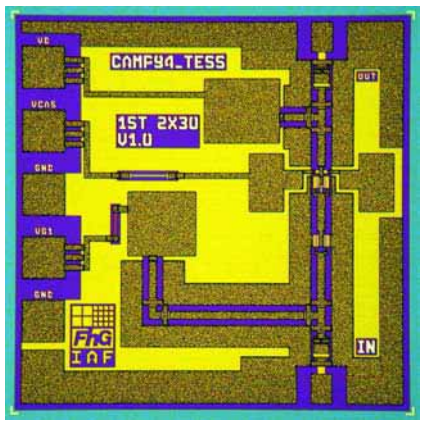


*Fig. 6. 94 GHz low-noise amplifier MMIC in cascode configuration. Chip-size 1 x 1 mm$^2$.*

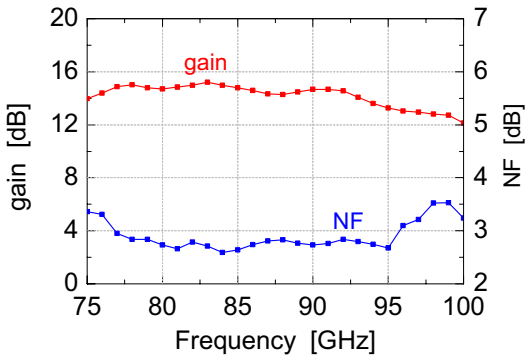


*Fig. 7. On-wafer measured gain and noise figure of the 94 GHz cascode low-noise amplifier MMIC. A noise figure of 2.8 dB between 80 and 95 GHz is achieved.*

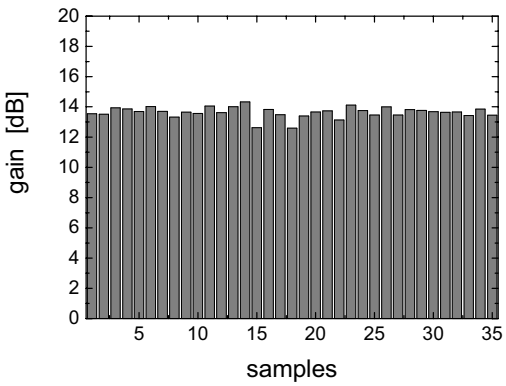


*Fig. 8. Low-noise amplifier gain at 94 GHz for all 35 chips on wafer revealing high uniformity, and yield.*

Following the same circuit design approach, a two-stage cascode amplifier MMIC (Fig. 9) for operation in D-Band was developed. As shown in Fig. 10, a high gain of 15 dB at 160 GHz is achieved [6].

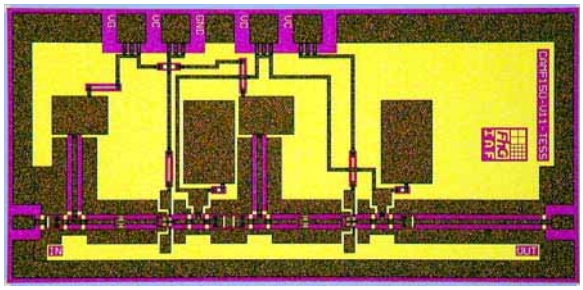

*Fig. 9. D-Band amplifier MMIC. Chip size 1 x 2 mm²*

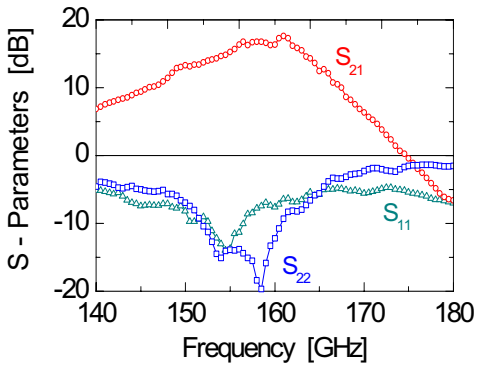


*Fig.10. On-wafer measured S-Parameters of D-Band amplifier MMIC.*

High speed frequency dividers are key elements in a wide range of mixed-signal applications, such as high speed data transmission systems or frequency synthesizers. Static 2:1 frequency dividers in SCFL logic [7] yielding an operation frequency of 70 GHz at only 450 mW power dissipation, and 108 GHz dynamic 2:1 frequency dividers were realized using the E-MHEMT technology [8]. To our knowledge, these are the highest operation frequencies obtained for frequency dividers in HEMT technology. The yield obtained for the static frequency divider with approximately 100 active devices was 70 %. Fig. 11 shows a photograph of the static frequency divider chip.

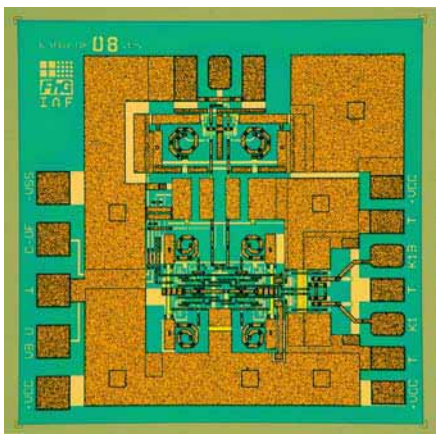

*Fig. 11. 2:1 static frequency divider chip for operation up to 70 GHz. Chip-size 1 x 1 mm².*

## V. Conclusion

The 70 nm metamorphic HEMT process with extrinsic cut-off frequencies of $f_t = 293$ GHz and $f_{max} = 337$ GHz developed at the IAF proved its usability for low-noise amplifier MMICs, showing high yield both at the transistor, and circuit level. The demonstrated transistor lifetime under bias in air is $1x10^6$ hours. The noise figure of the 80 to 95 GHz LNA IC is 2.8 dB which is comparable to the best values published for InP-based HEMTs. An amplifier MMIC developed for D-Band operation features a gain of 15 dB at 160 GHz.

The 100 nm enhancement MHEMT process demonstrated its usability for high-speed digital circuits. The measured maximum toggle frequencies of 70 GHz for the static 2:1 frequency divider, and 108 GHz for the dynamic 2:1 frequency divider are comparable to the best results achieved in SiGe or III/V-HBT technology.

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