ICs for 100 Gbit/s Data Transmission

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***Abstract* — Research and development of InP-based transistors and integrated circuits (ICs) are driven by applications in millimeter-wave wireless and broadband optical fiber communications systems. This paper describes our research activities on InP HEMT and HBT IC technologies for optical communications systems and discusses the future prospects and technical issues of ICs for 100 Gbit/s and beyond.**

I. Introduction

IC technology has contributed to the development of economical high-speed optical communications systems. Up to now, 40-Gbit/s SONET/SDH [1] and OTN [2] frame formats have been standardized for telecommunications systems, while 10-Gbit/s Ethernet has been standardized for data communications systems. The interface speeds of telecommunications and data communications systems have increased by a factor of 4 and 10, respectively. This means that, if current trends continue, the next-generation interface speeds will be 160 Gbit/s for the former and 100 Gbit/s for the latter. Work on the technological aspects of 40-Gbit/s ICs has reached the stage where cost-effective commercial products are being developed, and dominant competing technologies are InP HBT and SiGe HBT in this area. The possibility of realizing 100-Gbit/s class ICs based on InP HEMTs and InP HBTs for next-generation systems is now being investigated.

This paper describes recent progress in our InP-based IC technologies and discusses their future prospects. After overviewing the optical transmission front-end ICs, we present the current status of our InP HEMT and InP HBT device technologies with some of our latest IC results and also discuss future prospects of IC technologies for 100-Gbit/s and beyond.

II. Overview Of Optical Transmission Front-End ICs

Figure 1 shows an example of the basic transmitter and receiver configurations. The clock multiplier unit (CMU) and the clock and data recovery circuit (CDR) are usually based on a phase-locked loop consisting of a voltage controlled oscillator (VCO), a phase comparator, a low pass filter, and a D-type flip-flop (D-FF). Analog ICs in the receiver like the transimpedance amplifier (TIA) and limiting amplifier (LIM) are generally required for 70 % bandwidth of the data rate with flat phase characteristics [3], while the modulator driver (DRV) in the transmitter requires both broadband characteristics

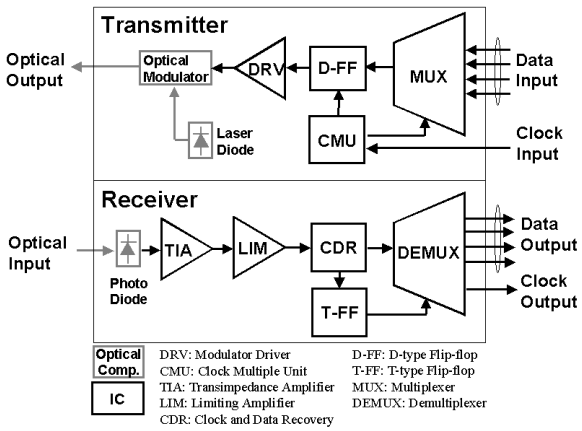


Fig. 1. Basic transmitter and receiver configurations.

and high saturation output power. As for digital ICs, such as multiplexer (MUX) and demultiplexer (DEMUX), switching operation at the data rate is required. Figure 1 shows an example of a full-rate system, which means the D-FF and CDR operate at the data rate with a clock signal that is the same as the data rate. In this system, the D-FF and CDR are critical components, and they limit system speed because of their full-rate clock operations. A system in which the D-FF is eliminated and CDR operates with the half the data-rate clock (referred to here as a half-rate system) mitigates the speed requirement for the electrical components. The full-rate system is, however, superior to the half-rate system in the system margin and robustness. Up to now, basic 100-Gbit/s front-end ICs, such as baseband amplifiers [4,5], a static frequency divider [6], MUX [7,8], and VCO [9,10], have been demonstrated. Dominant technologies in 100-Gbit/s-class ICs are currently InP-based HEMT and HBT.

III. Current Status Of NTT's InP-Based ICs

A. InP HEMT ICs

We have developed InP-based HEMT IC technology for 40-Gbit/s optical communications systems. The IC integrates 0.1-μm-gate-length InAlAs/InGaAs/InP HEMTs, InAlAs Schottkey diodes, metal resistors, MIM capacitors, and two-level interconnection lines with a low-permitivity interlayer [11]. Typical average threshold voltage is – 0.5 V, and the standard deviation is low at around 13 mV for a 3-inch wafer. The typical transconductance (gm) is 1.2 S/mm, and the current gain cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) are 186 and 320 GHz, respectively.

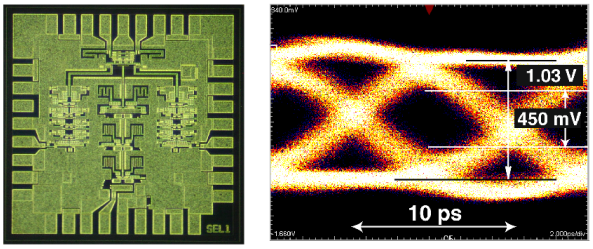
Table 1 summarizes the performance of the 40-Gbit/s InP HEMT ICs [12]. We have developed a TIA, a LIM, distributors for data signal and clock signal, a fully monolithic integrated CDR, a D-FF, a T-type flip-flop (T-FF), and a low-power 4-bit MUX and DEMUX to construct the optical transmitter and receiver shown in Fig. 1. The analog ICs offer sufficient performance for 40-Gbit/s applications, while the digital ones exhibit error-free operation at up to 50 Gbit/s. All of the 40-Gbit/s electrical components except for the modulator driver can be made by using InP HEMT technology. Reliability tests have already been performed for small-scale ICs, and the lifetime of the T-FF IC is 1 x 10^6 h at the junction temperature of 100 degrees centigrade [13].

To investigate the possibility of making 100-Gbit/s-class ICs, we first examined the multiplexing operation of a 2-bit MUX and the demultiplexing one of a D-FF using the InP HEMTs. To boost MUX circuit speed, we devised a selector core so that it can directly drive the external 50-Ω load. Figures 2(a) and (b) show a chip photograph of the MUX IC and its operating waveform at 100 Gbit/s. Clear eye opening is obtained with the output voltage of 1.03 V and the eye height of 450 mV. Error-free operation for a 2^{23}-1 PRBS signal is also confirmed at 100 Gbit/s by using a test chip that contains the MUX and the D-FF. These results confirm that both the 100-Gbit/s multiplexing operation of the MUX IC and the 100-Gbit/s demultiplexing operation of the D-FF were successfully achieved [7]. The current 0.1-μm-gate-length InP HEMT has a potential to construct half-rate 100-Gbit/s systems.

TABLE 1
PERFORMANCE OF INP HEMT ICS

Circuit	Operating Speed	Output (V_{pp})	Power (W)
TIA	Zt= 48.2 dBΩ, f_{3dB}= 43 GHz	0.46	0.35
Limiting Amp.	Gain= 25.4 dB, f_{3dB}= 32 GHz DC - 50 Gbit/s, Sens.: 27 mV @43G	1.3	0.6
Distributors	Data: DC - 50 Gbit/s	1.1	1.6
	Clock: 2 - 47 GHz	1.0	0.5
CDR	43 Gbit/s, Sens.: 175 mV	1.2	2.8
D-FF	20 - 50 Gbit/s P.M.: 101 deg. @50G	0.9	1.7
T-FF	8 - 50 GHz	0.8	1.1
4-bit MUX	7 - 50 Gbit/s P.M.: 170 deg. for 12.5-G input	1.0	1.7
4-bit DEMUX	4 - 50 Gbit/s Sens.:235 mV, P.M.:234 deg.@50G	0.53	1.4

Sens.: Input Sensitivity
P.M.: Phase Margin



(a) (b)

Fig. 2. 100-Gbit/s InP HEMT 2-bit MUX IC.
(a) Chip photograph (chip size: 2 mm x 2 mm).
(b) Operating waveform at 100 Gbit/s.

B. InP HBT ICs

Table 2 shows NTT's InP HBT technology roadmap. The first-generation HBT (G1) has an emitter width of 2 μm. The f_T and f_{max} are around 100 GHz and 150 GHz, respectively, at collector current density of 0.5 mA/μm^2. The second-generation HBT (G2) has been developed for 40-Gbit/s ICs. It has an emitter width of 1.0 μm and a C-doped base structure to improve reliability. The G2 HBT [14] also has undoped-emitter structure to reduce the power consumption of ICs; it exhibits higher f_T at lower collector current than the conventional n-doped emitter structure [15]. The typical f_T and f_{max} of HBTs are around 150 GHz and over 200 GHz, respectively. The third-generation HBT (G3) is being investigated for full-rate 100-Gbit/s ICs. It has an emitter width of around 0.6 to 0.8 μm. To achieve high f_T and f_{max} of over 300 GHz, the base and collector layers have been thinned to 30 and 150 nm, respectively. This device has the record f_T value of 341 GHz [16].

Table 3 summarizes performance of our InP HBT 40-Gbit/s digital ICs using G2 HBTs [17]. A master-slave type D-FF (MS-D-FF), a 4-bit MUX, and a 4-bit DEMUX operate at up to 50 Gbit/s, and a 16-bit MUX also has sufficient speed margin for 40-Gbit/s applications. A full-rate monolithic CDR operates at 40 Gbit/s. To access circuit-level high-speed performance using the G2 HBTs, we designed and fabricated a dynamic 1/8-frequency divider [18] and a selector IC [19]. The dynamic frequency divider operates at 90 GHz and the selector IC operates at 86 Gbit/s. As for G3 devices, we have confirmed 100-GHz operation of a clocked-inverter type dynamic 1/2-frequency divider and 100-Gbit/s operation of a selector IC. Figure 3 shows a

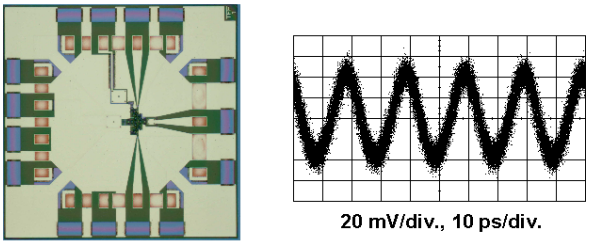
TABLE 2
TECHNOLOGY ROADMAP OF NTT'S INP HBT

Parameter	1st Generation	2nd Generation	3rd Generation
Epitaxial Growth	MOCVD	MOCVD	MOCVD
Base Doping	Zn	C	C
Emitter Width	2 μm	1.0 μm	0.8 μm
Base Thickness	50 nm	50 nm	30 nm
Doping	4 x 10^{19} cm^{-3}	4 x 10^{19} cm^{-3}	6.0 x 10^{19} cm^{-3}
Sheet Resistance	600 Ω/□	600 Ω/□	600 Ω/□
Collector Thickness	300 nm	300 nm	150 nm
Current Density	0.5 mA/μm^2	1.0 mA/μm^2	5.0 mA/μm^2
f_T	~ 100 GHz	~ 150 GHz	> 300 GHz
f_{max}	~ 150 GHz	~ 250 GHz	> 300 GHz

TABLE 3
PERFORMANCE OF INP HBT ICS

Circuit	Operating Speed	Power (W)
D-FF	50 Gbit/s	0.75
CDR	40 Gbit/s	1.7
4-bit MUX	50 Gbit/s P.M.: 180 deg. for 12.5-G input	2.5
4-bit DEMUX	50 Gbit/s P.M.:140 deg.@50G	2.6
16-bit MUX	47 Gbit/s	3.2

P.M.: Phase Margin



(a) (b)

Fig. 3. 100-GHz clocked-inverter 1/2 dynamic frequency divider IC.
(a) Chip photograph (chip size: 1.5 mm x 1.5 mm).
(b) Output waveform at 100-GHz IC operation.

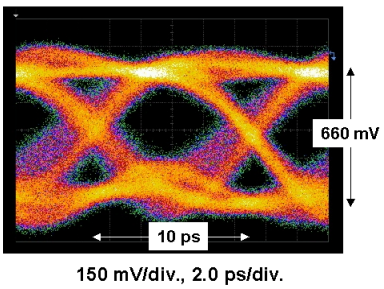


Fig. 4. Output waveform of the 100-Gbit/s InP HBT selector IC.

chip photograph and output waveform of the dynamic frequency divider, while Fig. 4 shows the 100-Gbit/s output waveform of the selector IC. As for a full-rate MS-D-FF, circuit simulations show that the D-FF can operate at 100-Gbit/s.

IV. Prospects Of 100 Gbit/s And Beyond

It is important to clarify the transistor performance required for full-rate 100-Gbit/s and 160-Gbit/s circuit operations. Figures 5 and 6 show the propagation delay (*tpd*) contours of source-coupled FET logic (SCFL) [20] and emitter-coupled logic (ECL) [21], respectively. The performance of state-of-the-art devices is also plotted in these figures. In Fig. 5, it should be noted that the parasitic capacitance is assumed to half that of the state-of-the-art NTT devices. The maximum operating speed of a full-rate MS-D-FF is empirically given by $1/(3.3\ tpd)^{-1}$ [22]. The delay times should therefore be lower than 3 ps/gate for a 100-Gbit/s MS-D-FF operation and lower than 2 ps/gate for a 160-Gbit/s one. For FET devices, an f_T of over 280 GHz and a *gm* of over 1.4 S/mm are needed for 100 Gbit/s, and an f_T of over 440 GHz and a *gm* of over 1.9 S/mm are required for 160 Gbit/s. Although dynamic circuit configurations like super-dynamic flip-flop [3] relax these requirements, novel device technologies should be developed. To satisfy the requirement for 100 Gbit/s, reduction of parasitic capacitance (half that of our current InP HEMT), shortening the gate length (~50 nm) and thinning the barrier layer (~10 nm) are necessary [20]. As for HBT devices, our G3 HBT as well as some other reported HBTs have a potential of achieving 100-Gbit/s D-FF operation, as shown in Fig. 6. For 160-Gbit/s MS-D-FF operation, an f_T of around 400 GHz and an f_{max} of around 500 GHz will be required. To achieve this device performance, emitter width and base and collector thickness should be further scaled down [23].

To construct 100- and 160-Gbit/s transmitters and receivers, we need not only high-speed ICs but also packaging technology covering 100-GHz bandwidth. The need for packaging technology can be alleviated by monolithic integration of optical components and electronic devices. In this case, all functions for receivers and transmitters shown in Fig. 1 should be integrated to make the electrical interface speed lower than the currently available bandwidth (~65 GHz). As for the optical receiver, we have demonstrated a full-rate 40-Gbit/s optoelectronic decision IC [24] integrated with a uni-traveling carrier photodiode [25] and the 0.1-µm-gate-length InP HEMTs. The photodiode has over 100-GHz-class bandwidth and high-saturation output power. The fusion of high-speed optical device and functional ICs will be the key for beyond 100-Gbit/s.

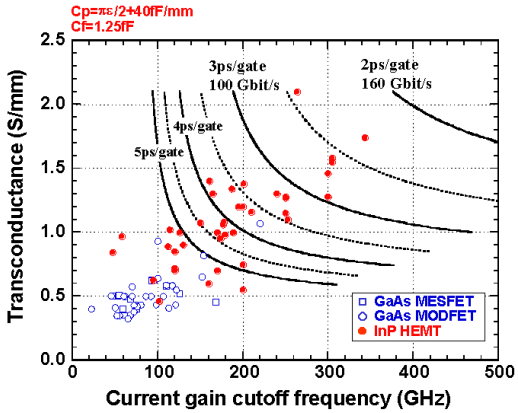


Fig. 5. Propagation delay contours of SCFL inverters.

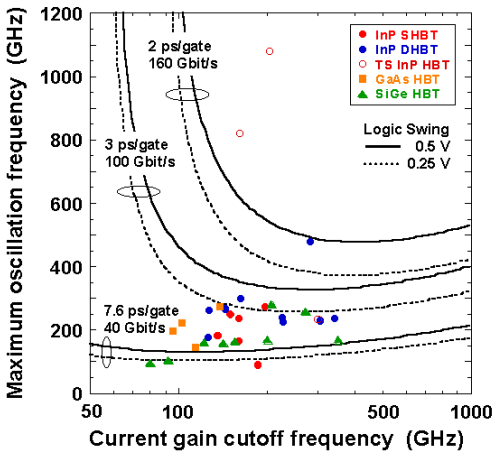


Fig. 6. Propagation delay contours of ECL inverters.

V. Conclusion

We reviewed our InP-based IC technologies for optical communications systems. 40-Gbit/s ICs have been developed using the 0.1-µm-gate-length InP HEMT technology. A selector and D-FF using the InP HEMT operate at 100 Gbit/s, which indicates that this HEMT

technology has a potential to construct 100-Gbit/s half-rate clock systems. A 1.0-μm-emitter-width InP SHBT technology has also been developed for 40-Gbit/s MSI-class low-power digital ICs. The next-generation 0.8-μm-emitter-width InP DHBT is being investigated for future full-rate 100-Gbit/s class ICs. InP-based optoelectronic IC technology will play an important role in overcoming the bottleneck of electrical interconnection.

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