Large-Signal Modeling of SiGe HBTs Including a New Substrate Network Extraction Method

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***Abstract*—Large-signal modeling results of SiGe HBTs with HICUM (High Current Transistor Model) are presented. Moreover, a new and robust method to determine the substrate network elements of bipolar transistors from S-parameter measurements is proposed in this work. The investigated substrate network is compatible with HICUM and includes the substrate-collector depletion capacitance, substrate resistance and capacitance.**

I. INTRODUCTION

WITH the introduction of SiGe into the base, bipolar transistors have achieved a tremendous improvement in their operating frequencies and current gain. As a consequence of this improvement and reduced transistor dimensions, the demands for more accurate and broadband transistor models can only be met with more complicated and up-to-date transistor models which cover a wide frequency and bias range. The parasitic effects associated with the isolation layers, the substrate and the distributed characteristics of the base-emitter and base-collector junctions are taken into account in HICUM (High Current Transistor Model) improving the modeling of the RF transistor operation up to our upper measurement frequency limit, 40 GHz. A detailed description of the outstanding features of HICUM can be found in [1].

This paper is organized as follows. In the second section DC and RF modeling and measurement results of a SiGe HBT (Heterojunction Bipolar Transistor) will be presented. The modeling accuracy will be discussed by means of the high frequency linear and nonlinear measurements besides the conventional DC measurements. In the third section, a new substrate network extraction method will be introduced and its compatibility with HICUM will be investigated. The substrate network consists of the substrate-collector depletion capacitance, the substrate resistance due to the resistivity, and the substrate capacitance due to the permittivity of the substrate. The analytically derived equations enable a fast and accurate extraction of the substrate network elements from simple S-parameter measurements. The parameter extraction of the substrate network takes place in different frequency regions, since each substrate network element governs the high frequency output admittance of the transistor in a certain frequency range. $\mathrm{Re}(Y_{22}+Y_{12})$ falls off with increasing frequency owing to the existence of the substrate capacitance C_{sub} connected parallel to the substrate resistance R_{sub}. From this fall-off C_{sub} can be analytically obtained. This phenomenon will be explained in detail in Section III.

II. DC AND RF MODELING AND MEASUREMENT RESULTS

The device under test is a SiGe HBT from AMI Semiconductor with an emitter length of 9.4 μm in common-emitter configuration. All the devices have a single emitter finger and a grounded substrate contact. DC characteristics of the transistor were measured using an Agilent 4155 Semiconductor Parameter Analyzer and the S-parameters were measured using an HP 8510 Network Analyzer. The high frequency nonlinear and noise characteristics of the transistor were measured using an HP 70820 Microwave Transition Analyzer and an HP 8970 in conjunction with a mechanical tuner to adjust the source reflection coefficient seen by the transistor, respectively. The DC measurement and modeling results can be viewed in Fig. 1. The weighting factors available as model parameters have been optimized to model the base-width modulation accurately.

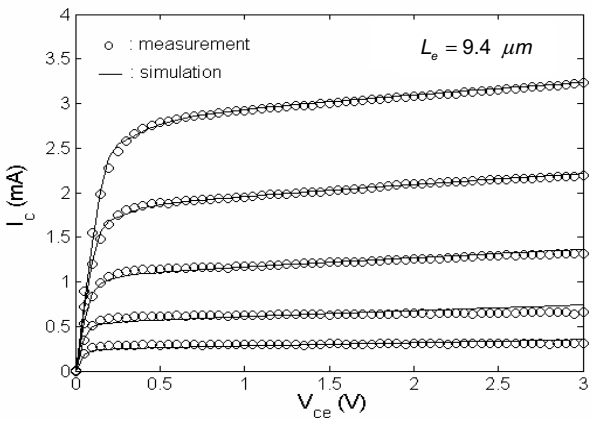


Fig. 1. Measured and simulated DC characteristics of the SiGe HBT

The large-signal measurement and simulation results performed for a fundamental tone of 2 GHz are illustrated in Fig. 2. P_{in} denotes the RF power at the transistor input. The fundamental tone can be accurately predicted whereas the measured third harmonic tends to deviate from the simulated curve for small input powers which is attributed to the limited dynamic range of the transition analyzer.

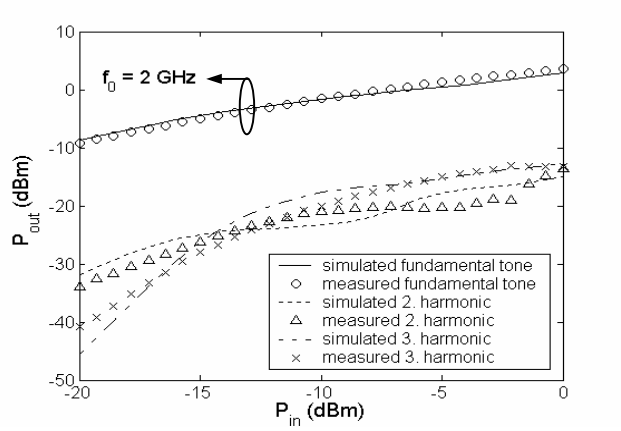
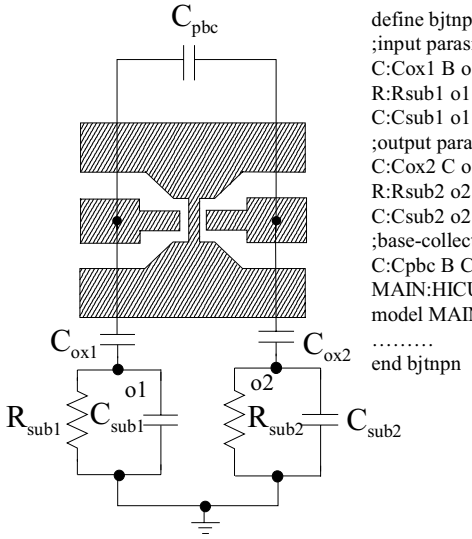


Fig. 2. Simulated (with pads) and measured large-signal characteristics of the SiGe HBT

To take into account the parasitics associated with the contact pads, the transistor model has been extended by the equivalent circuit of the contact pads as can be seen Fig. 3. The base-collector coupling capacitance C_{pbc} has a negligible effect on the large-signal simulation results of the investigated transistor.




```
define bjtnpn (C B E S )
;input parasitics
C:Cox1 B o1 C=112E-015
R:Rsub1 o1 E  R=93
C:Csub1 o1 E  C=30E-015
;output parasitics
C:Cox2 C o1 C=116E-015
R:Rsub2 o2 E  R=90
C:Csub2 o2 E  C=43E-015
;base-collector coupling
C:Cpbc B C C=2.2E-015
MAIN:HICUM C B E S 0
model MAIN HICUM \
……
end bjtnpn
```

Fig. 3. Equivalent circuit of the contact pads used for large-signal simulations. This circuit has been implemented using the *hpeesof* simulator in ICCAP of Agilent.

The measured and simulated S-parameters for a typical operating point ($V_C = 1.5\ V$ and $J_C = 0.18\ mA/\mu m^2$), where the collector current density has been optimized for a low minimum noise figure, are shown in Fig. 4. The measured S-parameters have been de-embedded using the two-step de-embedding method with open and short test structures [2]. This de-embedding procedure shifts the measurement reference planes from the *GSG* on-wafer probe tips to the actual transistor reference planes.

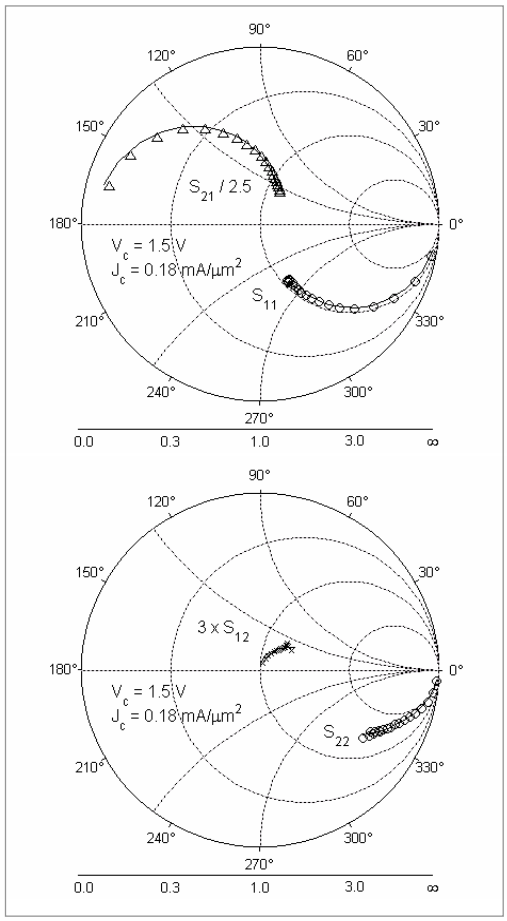


Fig. 4. Measured and simulated S-parameters of the SiGe HBT with an emitter length of $9.4\ \mu m$ ($freq = 1 - 40\ GHz$).

Noise parameters of our reference transistor with an emitter length of $9.4\ \mu m$ have been measured at 5 GHz with a mechanical tuner using the *Cold-Source Technique* [3]. Fig. 5 shows the associated gain and the measured and simulated minimum noise figure at different biases. The model predicts the minimum noise figure of the transistor at low current densities in Fig. 5 accurately whereas the agreement between the measurement and the simulation has been found to be slightly degraded at higher current densities. This is attributed for the time being to the interaction of the second stage noise contribution of the noise parameter measurement setup due to a lower transistor gain and a slight deviation of the extracted parameter values describing the high current operation [4] of the transistor from their physically correct values.

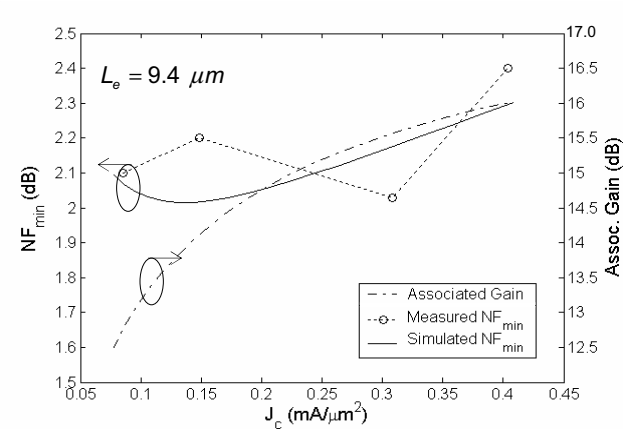


Fig. 5. Measured and simulated minimum noise figure and associated gain at 5 GHz

The thermal noise contribution and the power loss due to the contact pads add to the measured minimum noise figure of the transistor and therefore have been subtracted from the noise correlation matrix of the transistor using the noise and electrical transformation matrices [5], [6]

$$C_A = 2kT\begin{bmatrix} R_n & \frac{F_{\min}-1}{2} - R_n Y_{opt}^{*} \\ \frac{F_{\min}-1}{2} - R_n Y_{opt} & R_n \mid Y_{opt} \mid^2 \end{bmatrix} \quad (1)$$

where C_A is the noise correlation matrix and $F_{\min}$, Y_{opt} and R_n are the measured noise parameters.

III. SUBSTRATENETWORK

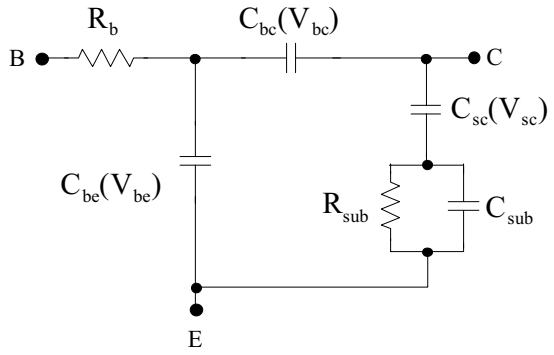


Fig. 6. Equivalent circuit of the npn-transistor under the cutoff operation with the substrate connected to the ground

In Fig. 6, the equivalent circuit of the transistor under the cutoff operation is illustrated. With the substrate node being connected to the ground, the substrate-collector depletion capacitance becomes a function of only the applied collector voltage and can be generally expressed as

$$C_{sc} = \frac{C_{sc0}}{\left(1 - \frac{V_{sc}}{V_{sc\phi}}\right)^{m_{sc}}}. \quad (2)$$

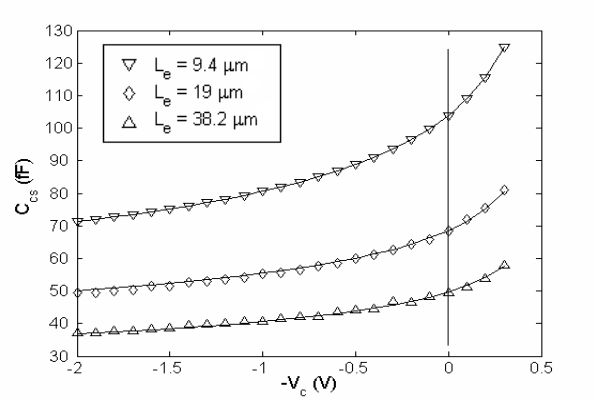


Fig. 7. Calculated (solid line) and measured (shapes) C_{sc} versus collector voltage for three transistor lengths ($V_b = -0.5\ V$, $freq = 1.9\ GHz$

C_{sc} and R_{sub} can be calculated by

$$C_{sc} = \mathrm{Im}(Y_{22} + Y_{12})/\omega \quad (3)$$

$$R_{sub} = \mathrm{Re}(Y_{22} + Y_{12})/\left(\mathrm{Im}(Y_{22} + Y_{12})\right)^2 \quad (4)$$

provided that $G_{sub}{}^2 >> \omega^2 (C_{sc} + C_{sub})^2$.

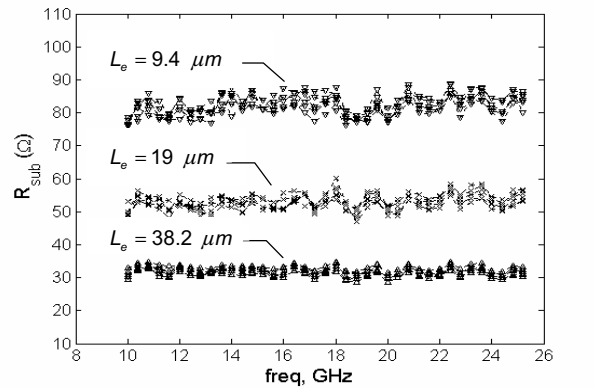


Fig. 8. Extracted substrate resistance R_{sub} for three transistor emitter dimensions ($V_b = -0.5\ V$, V_c varied between 2 and 1.5 V).

Having determined C_{sc} and R_{sub}, C_{sub} can be calculated by

$$C_{sub} = \sqrt{\frac{\omega^2 G_{sub} C_{sc}^2(V_{sc}) - G_{sub}^2}{\frac{\mathrm{Re}(Y_{22} + Y_{12})}{\omega^2}}} - C_{sc}(V_{sc}) \quad (5)$$

where $G_{sub} = 1/R_{sub}$. The substrate-collector capacitance C_{sc} has been written in (5) as a function of V_{sc} to emphasize the bias-dependence of C_{sc}.

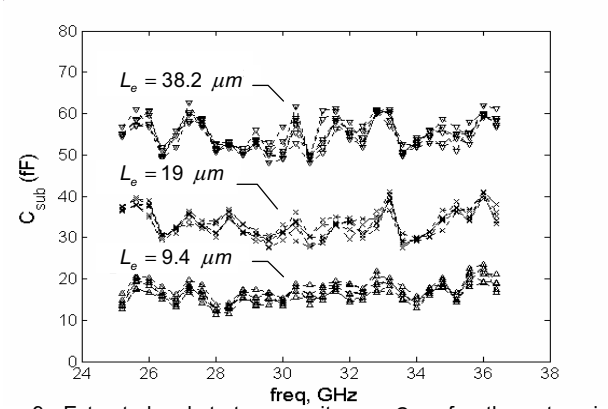


Figure 9. Extracted substrate capacitance C_{sub} for three transistor dimensions ($V_b = -\ 0.5\ V$, V_c varied between 2 and 1.5 V).

As a result, C_{sub} is extracted in the highest frequency range where (5) has somewhat a flat frequency response. This lies in the fact that the influence of C_{sub} on

$$\mathrm{Re}(Y_{22} + Y_{12}) = \frac{\omega^2 C_{sc}^2 G_{sub}}{G_{sub}^2 + \omega^2 (C_{sc} + C_{sub})^2} \qquad (6)$$

becomes critical due to an increase in the denominator of (6) with increasing frequency from which (5) is derived. The accuracy of the method can be verified by comparing the simulated and measured Y_{22} of the transistor in the forward-active mode. The HICUM model

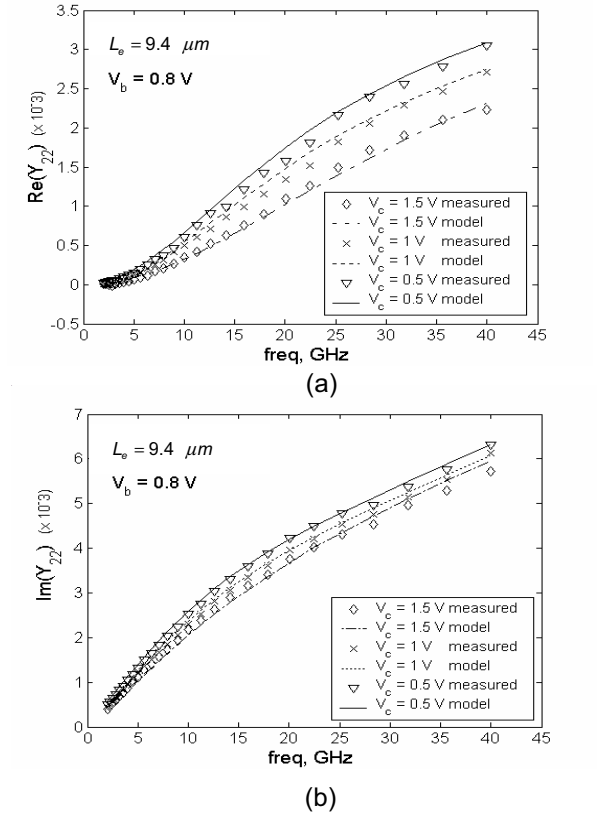


Figure 10. Measured and modeled (a) real and (b) imaginary part of Y_{22} for collector voltages between 0.5 and 1.5 V up to 40 GHz.

yields good results up to 40 GHz as shown in Figures 10a and 10b.

TABLE I
EXTRACTED SUBSTRATE RESISTANCE AND CAPACITANCE VALUES FOR THREE TRANSISTOR GEOMETRIES

Emitter Length	9.4 μm	19 μm	38.2 μm
R_{sub}	83 Ω	52 Ω	30 Ω
C_{sub}	17 fF	32 fF	56 fF

IV. CONCLUSIONS

DC and RF modeling results of SiGe HBTs with HICUM (High Current Transistor Model) have been presented. The model accuracy has been verified by DC, S-parameter and noise parameter measurements. Moreover, a new analytical direct extraction method to determine the substrate network parameters has been presented. The suggested extraction procedure has been successfully applied to the HICUM model. The investigated substrate network can accurately model the substrate effects up to 40 GHz and takes into account both resistive and dielectric behavior of the substrate.

ACKNOWLEDGMENTS

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