Power HBT reliability for space applications

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Abstract — **High power HBT process developed by UMS for X-band application have been space evaluated under CNES and ESA funding. The reliability assessment plan features high temperatures storage tests, DC life-tests, RF step test stress, ESD and radiation tests. A set of evaluation test vehicles was defined for this purpose. Activation energy have been determined, failure rate calculations are in line with the space requirements**

I. INTRODUCTION

UMS has developed an industrial GaInP/GaAs HBT process especially dedicated to high power MMIC amplifiers for applications from C to Ku frequency bands [1]. This process (HB20P) has been optimised for high reliability and includes specific features for reducing the junction temperature and increasing the thermal stability of the devices.

In order to demonstrate the ability of HB20P to meet the space requirements, an evaluation was initiated and funded by CNES and ESA.

The work involved in this evaluation consisted in:

- Documenting the process in a "Process Identification Document",
- Performing a quality survey of the manufacturing capability,
- Assessing the reliability of the components of the technology.

The presentation given here describes the work done in the frame of the reliability assessment of HB20P.

II. HBT PROCESS

The HB20P process is using 4'' GaInP/GaAs HBT epitaxial wafers; the transistors have a traditional multi-mesa configuration. Selective etching steps are used extensively, resulting in excellent uniformity and reproducibility of the critical parameters. The intrinsic excellent reliability is obtained thanks to the use of high quality GaInP/GaAs MO-CVD epitaxies; a depleted ledge layer passivation of the extrinsic emitter-base junction; non-alloyed metals are used for the emitter (refractory) and base ohmic contacts. We have developed an original technique for improving the thermal stability of multi-finger power transistors; a resistive layer is inserted in the epitaxial structure of the emitter, providing a built in ballast resistance in each emitter finger. The value of these ballast resistances has been optimised to prevent thermal run away (the so-called 'current-crunch' effect) and not to degrade significantly the microwave gains of the transistors. These integrated emitter ballast resistances avoid the use of bulky external base ballast resistances and decoupling capacitors, which would be otherwise mandatory for thermal stability. Finally, a thick gold metal layer is used to interconnect the emitter fingers and provide an efficient heat removal from the active area (see Fig. 1). The heat is extracted from the top emitter contacts, is transported by the high conductivity gold interconnect and is dissipated through the substrate far away from the active intrinsic junctions of the transistors. These gold thermal drains reduce significantly the junction temperatures and contribute dramatically to the thermal stability of the devices.

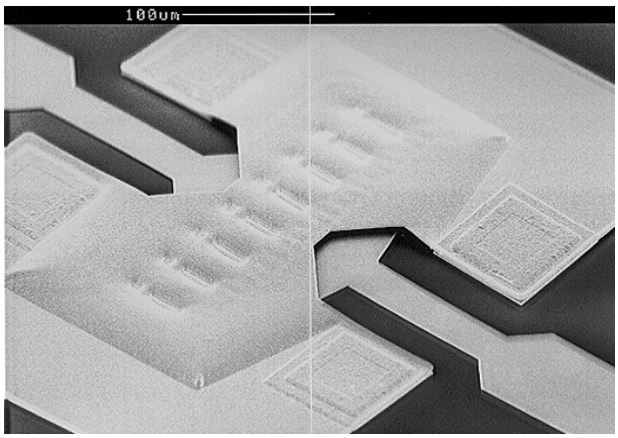

Fig. 1: SEM photo of a multi-finger X-band power HBT featuring the thick gold thermal drain covering the transistor.

During manufacturing, 20 Process Control Monitor (PCM) modules per wafer are measured; more than 100 parameters are extracted, to monitor and guaranty the stability and reproducibility of the process. At the end of wafer front-face processing, the [S] parameters of the single finger coplanar transistors of the PCM are measured; the RF performances of these control transistors are a part of the measured parameters for the final acceptance of the wafers.

III. HB20P TEST STRUCTURES

Three tests structures were designed in the frame of the evaluation. The first test structure is the "Technology Characterisation Vehicle" (TCV, see Fig 2) that is a set of elementary devices tailored to evidence degradation mechanisms. It comprises a transistor, resistances, via holes, MIM capacitor, inductor etc…This enables to track any degradation of each of the MMIC elements. Each element is independently biased at the maximum, or above the maximum rating. Only DC measurements can be made.

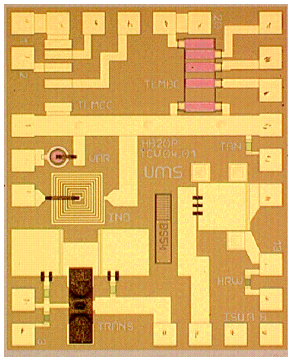

Fig. 2: TCV Structure.

The second test structure is the "Dynamic Evaluation Circuit" (DEC, see Fig. 3), which is formed by a very simple matched single stage amplifier operating at X-Band. Both DC and RF parameters are measured with DEC.

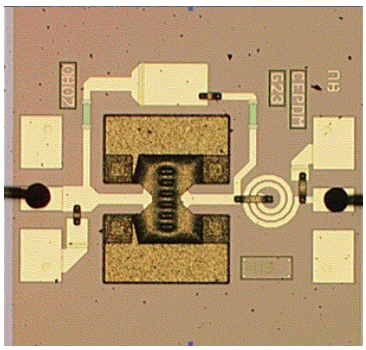

Fig. 3: DEC circuit.

The last test vehicle, the "Representative Integrated Circuit" (RIC, see Fig.3) is a two-stage high power amplifier at X-band. 8W of output power with an associated PAE of 40% has been achieved with this circuit.

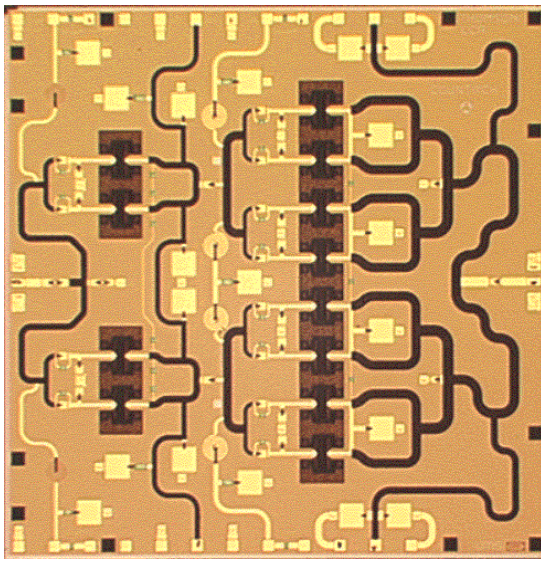

Fig. 4: RIC circuit.

IV. HB20P EVALUATION PLAN

The evaluation plan was defined with the following objectives:

- Determine the intrinsic wear-out mechanisms,
- Validate the capability domain of the technology,
- Evaluate the failure rate of a representative circuit.

The complete evaluation plan is given Fig 5.

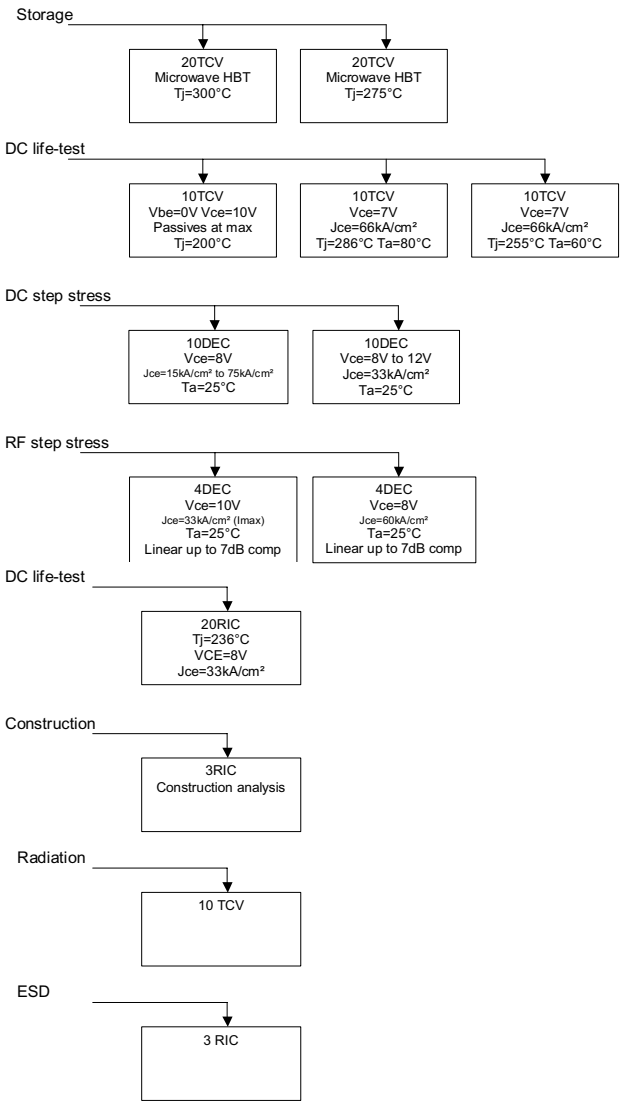

Fig 5 Evaluation test plan

It comprises a set of storage tests at high temperature (275°C and 300°C), intended to evidence diffusion related mechanisms, a series of DC current or voltage stress tests at high temperatures to determine activation energy versus temperature, a series of DC current and voltage step stress test to determine current and voltage maximum rating, a series of RF step stress test to determine the RF power maximum ratings and a DC life-test at high temperature is used for the RIC. In addition sensitivity to radiation and ESD has been evaluated.

All test vehicles are mounted in non-hermetic package. Wafers from different substrate suppliers were used.

V. TEST RESULTS

Storage test:

Degradation of the collector ohmic contact and base ohmic contact has been evidence. Activation energy of 1.94eV and 1.8eV has been calculated respectively. That mechanism is currently observed with gold-alloyed contact and is interpreted as resulting from a diffusion mechanism (Au into GaAs).

DC life-test

At high current density (50kA/cm²) and high temperature, current gain degradation is observed Fig (6). Previously to this space evaluation, tests at different current density gave a current acceleration factor of 1.9. Here activation energy in temperature of 1.36eV was found.

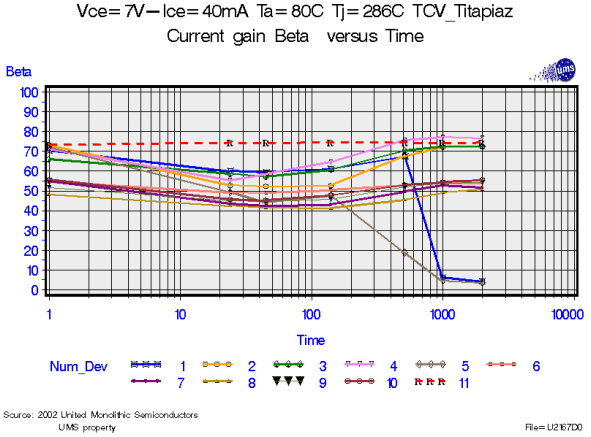

Fig. 6: Beta degradation

DC Step stress test:

Current gain degradation occurs above a collector emitter voltage of 10V associated to a current density of 33kA/cm² or for a current density of 60kA/cm² associated to VCE of 8V. We have also observed that devices with higher emitter resistance can sustain more current and voltage. We assume that current and voltage limitation are determined by the thermal runaway phenomenon .Fig (7)

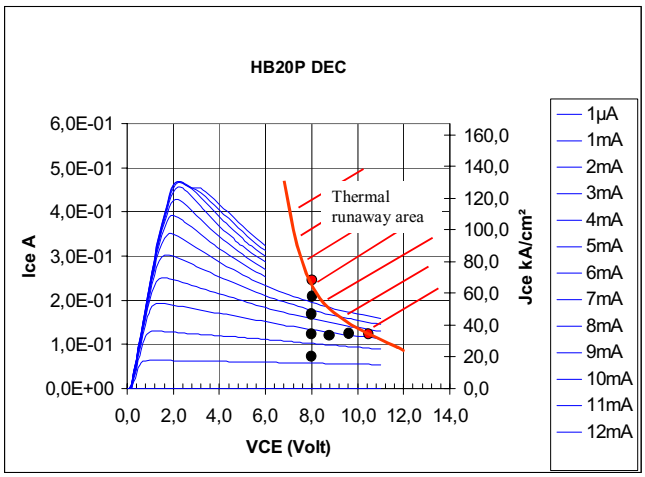

Fig.7: Current and voltage limitation

RF Step stress test:

DEC was biased at 10V and the input power is increase by step each week up to 7dB of gain compression, Fig (8). Devices with the lower emitter resistance (6 ohm for 1 finger of 2x30um) failed after 3dB of gain compression. Devices with higher emitter resistance (9 ohms for 1 finger of 2x30um) are still alive after 7 dB of gain compression.

Fig.8: Pout, current and gain versus time

RIC DC Life test:

4000 hours of tests have been done on an X-Band high power amplifier. This circuit was designed to operate in pulse mode at Vce=8V and Jce=33kA/cm² in large signal, with a maximum dissipated power of 10W. In this programme, RIC was biased in continuous DC mode without RF. Dissipated power was about 18,5W per chip and the junction temperature was 235°C. Several parts failed during the test, but mainly due to a bad assembly (voids in the solder between the chip and the carrier). However 11 parts reached 4000 hours without any drift and a Median Time to Failure (MTF or $t_{50\%}$) of 67 years is obtained at Tj = 175°C with an activation energy of 1,36eV.

ESD test:

Test has been performed on RIC according the human body model. Input capacitance in the RF port failed after 1kV and output capacitance failed at 400V (class 1). The transistor has not failed after 4kV (class 3) applied on the base or on the collector bias accesses. Those results are better than those in general given for GaAs devices [2] and are in agreement with those previously obtained on FET processes.

Radiation test:

Radiation tests were done to assess the sensitivity of the HB20P process to burn out caused by heavy ions. The approach decided was to test one component in the worse conditions (Particle with the highest energy, fluence of 10^7 particles/cm², bias Vce = 10 V and Vbe = 0V) The first step was done using Iodine ($_{127}$I, LET (Si) = 60 MeV/mg/cm²), which is the most energetic particle available on the equipment. No failure occurred at 200 MeV. The test was repeated at 256 MeV and again no failure occurred. This sequence was repeated on a second TCV without failures. Those results confirm the hardness of the process in blocked conditions (Vbe = 0), which is believed to be a worst case.

VI. Conclusion

HB20P intrinsic wear-out mechanisms have been characterized and activation energy have been determined. In storage a MTF above 110 years at 175°C has been deduced. From DC life-test a MTF above 440 years at a junction temperature of 175°C and at two times the standard current density has been determined. Current gain degradation is linked to current density and follows the black law with an **m** factor of 1,9. ESD tests were implemented showing that HB20P transistors are not more sensitive than other GaAs components.

The RF step stress test confirmed that the HB20P transistor with an emitter resistance of 9Ω (for 1 finger of 2x30µm²) can operate up to 7dB of gain compression level at Vce=10V and Jce=33kA/cm².
4000 hours of tests have been done on an X-Band high power amplifier, demonstrating an MTF above 67 years.
To our knowledge UMS HB20P is the first GaInP/GaAs HBT process suitable for high power applications that has been space evaluated.

Acknowledgement

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References

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