A 5GHz-Band On-Chip Matching CMOS MMIC Front-End

Hiro-omi Ueda[1], Shintaro Shinjo[1], Yasuhiro Nabeno[1], Masayoshi Ono[1],
Takahiro Ohnakado[2], Takaaki Murakami[2], Akihiko Furukawa[2], Yasushi Hashizume[2],
Kazuyasu Nishikawa[2], Takeshi Mori[2], Satoshi Yamakawa[2], Tatsuo Oomori[2] and Noriharu Suematsu[1]

[1] Information Technology R&D Center, Mitsubishi Electric Corp.,
Kamakura, Kanagawa, 247-8501, Japan
Tel:+81-467-41-2544 Fax:+81-467-41-2519, e-mail : h_ueda@isl.melco.co.jp

[2] Advanced Technology R&D Center, Mitsubishi Electric Corp.,
Tsukaguchi-Honmachi, Amagasaki, Hyogo 661-8661, Japan

***Abstract* — A 5GHz-band CMOS MMIC front-end is developed, which includes a two-stage power amplifier (PA) with a single-stage push-pull driver (DRV), a three-stage low noise amplifier (LNA), and a transmit/receive (T/R) switch. The high current on-chip matching spiral inductor is used for the on-chip matching PA. On-chip matching configuration enables these circuits to connect internally. The IC performs 14.8dBm transmit power, and 4.1dB receiver noise figure at 5.2GHz.**

I. INTRODUCTION

The broadband wireless communication systems such as Bluetooth and wireless LAN (802.11a/b/g) demand for low cost and single transceiver chip. Therefore, transceiver system on a chip using a sub-micron CMOS process has created considerable interest in recent years [1],[2]. However, it seems not easy to apply a standard CMOS technology to fully on-chip matched and fully integrated RF front-end circuits because of the main two reasons. These are follows; (1) the low breakdown voltage of transistors, (2) the miss-match loss originated from passive elements for matching circuits such as spiral inductors, interconnection lines, and so on.

In terms of (1) the low breakdown voltage of transistors, this is a disadvantage for power amplifier (PA). The drain-to-source voltage limitation of the sub-micron CMOS such as 0.18µm FET and 0.40µm FET is 1.8V and 3.3V, respectively. To obtain high power handling capability even in the case of low breakdown voltage CMOS FET's, the uses of a cascode configuration and a complementary push-pull configuration have been proposed [3]. In this study, we apply these configurations on the two-stage PA and the driver amplifier (DRV), and optimize the gate bias condition of cascode-stage to improve the power performance. In terms of (2) the miss-match loss, the circuit is designed using the equivalent circuit model of the passive elements which are extracted from the fitting to the measured S-parameters [4]. Additionally, we consider the interconnection lines as the transmission lines, and the circuit and layout design are optimized to reduce the matching loss in the post-layout simulation. The spiral inductor used as bias feed of a final-stage PA causes additional miss-match problem. The spiral inductor needs high current capacity and high-Q, but a conventional spiral inductor has low current capacity and low-Q. That involves a relatively large loss in matching circuits. In this study, we use a high current spiral inductor for a bias feed of the second stage PA to reduce the matching loss.

This paper describes the configuration and measured performance of the 5GHz-band CMOS MMIC front-end with fully monolithic matching circuits utilizing a 0.18µm CMOS process.

II. CONFIGURATION

Figure 1 shows the block diagram of CMOS MMIC front-end. This IC consists of a two-stage PA with a single-stage push-pull driver amplifier (DRV), a three-stage low noise amplifier (LNA), a transmit/receive (T/R) switch [5],[6], and their bias circuits. The PA and the LNA include the input, output, and all inter-stage matching circuits on chip, so as to connect the T/R switch internally.

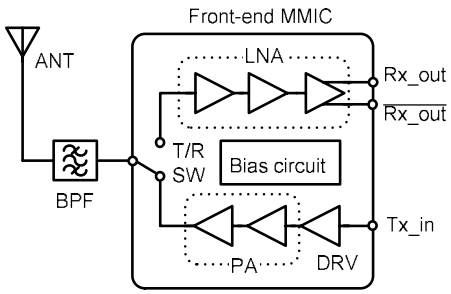

Fig. 1. Block diagram of CMOS MMIC front-end.

PA:

Figure 2 shows the schematic diagram of the two-stage PA. The cascode configuration is used for both stage PA's, to realize high gain and high power at 5.2GHz. The gate-width is optimized using a circuit simulation analysis for these stages. In the first stage, the gate-length of M11 is 0.18µm to realize high gain, and that of M12 is 0.40µm to improve the power handling. The gate-width of M11 and M12 are both of 400µm. In the second stage, the gate-length of both

M21 and M22 are 0.40µm to improve the power handling. The gate-width of M21 and M22 are 800µm and 600µm, respectively. The high current spiral inductor L3 is used stacked aluminum metal and the width of conductor is 30µm, and has current capacity of 100mA.

To obtain the high power performance of the sub-micron CMOS PA, the gate bias conditions of the cascode-stages are optimized. Setting the gate bias voltage of the cascode-stages lower than that of drain voltage, the maximum output power performance is obtained. At this bias condition, it is confirmed in simulation that the maximum voltage swing on drain-to-source at 1-dB gain compressed output power (OP_{1dB}) is within FET's voltage limitation.

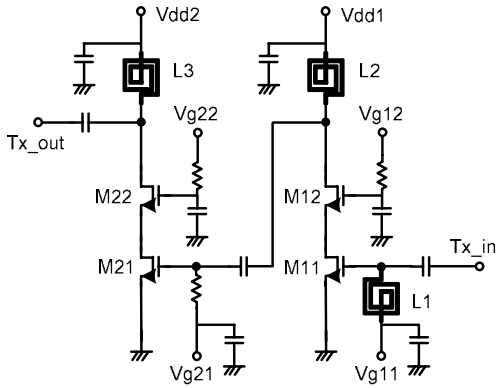

Fig. 2. Schematic diagram of two-stage PA.

LNA:

Figure 3 shows the schematic diagram of the three-stage LNA. The common-source configuration is used for the first-stage LNA's to improve the noise figure (NF). The gate-width is 200µm which is optimized to realize the lowest NF at 5.2GHz. The cascode configuration is used for the second-stage to realize high gain. The differential pair is used for the final-stage to translate to the differential input of the next stage for the mixer.

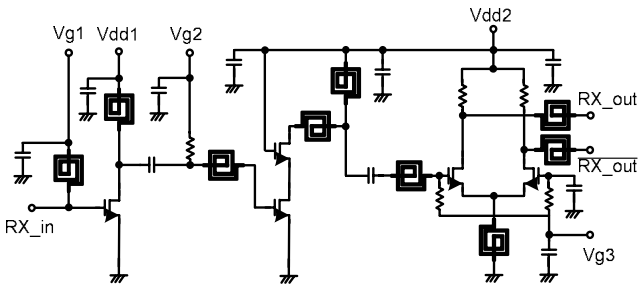

Fig. 3. Schematic diagram of three-stage LNA.

T/R switch:

Figure 4 shows the schematic diagram of T/R switch. A single-pole double-throw (SPDT) T/R switch is fabricated utilizing the Depletion-layer-Extended Transistor (DET) [5] in the 0.18µm CMOS process. A shunt/series type circuit is used to improve isolation characteristics at a high frequency of 5.2GHz. As a circuit topology, the source/drain (S/D) DC biasing scheme is used to improve power-handling capability. 1V is applied to S/Ds of all transistors ($V_{S/D}$=1V), and 2.8V and 0V are applied to V_{CTRL} and $V_{\overline{CTRL}}$. This voltage condition is determined with regard to power-handling capability enhancement and gate dielectric reliability limitation.

Figure 5 shows a photograph of fabricated CMOS MMIC front-end. The chip size is 2mm x 2mm, and the IC is fabricated in the 0.18µm CMOS process.

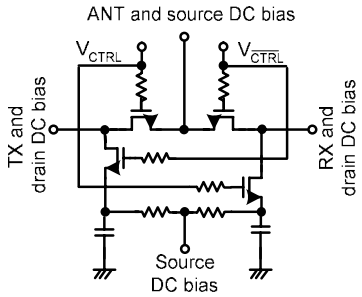

Fig. 4. Schematic diagram of T/R switch.

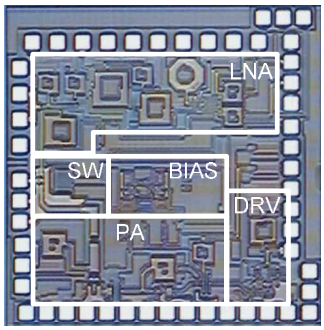

Fig. 5. Photograph of fabricated CMOS MMIC front-end.

III. MEASURED RESULTS

RF characteristics of the fabricated CMOS MMIC front-end are investigated on the individual circuits. Figure 6 shows measured return-loss and gain characteristics of the two-stage PA. The bias condition is Vdd1=3.0V, Vdd2=3.3V, Vg12=2.4V, Vg22=2.8V. The quiescent currents of the first and the second stage PA's are 25mA and 45mA, respectively. The first and second stages are class AB operation, and the gate bias conditions of the cascode-stages are optimized to obtain a high power performance. The input return-loss is 10dB and the output return-loss is 12dB at 5.2GHz. The gain of 8.7dB is obtained at 5.2GHz. The high current spiral inductor successfully reduces the matching loss.

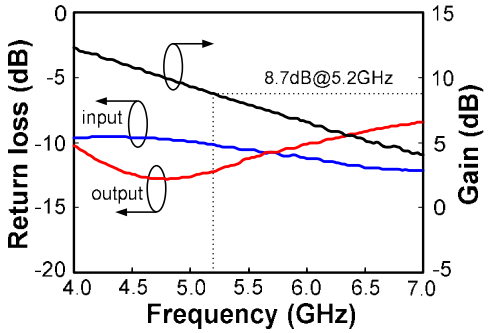

Fig. 6. Measured return-loss and gain characteristics of the PA.

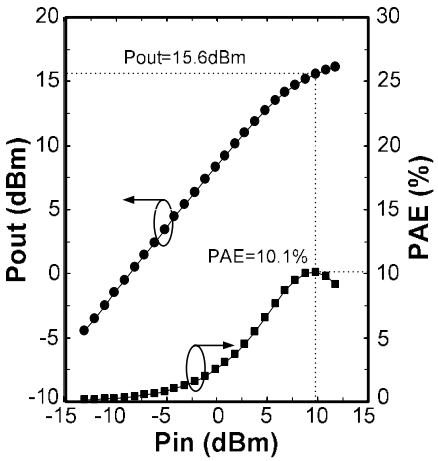

Fig. 7. Measured transfer characteristics of the PA

Figure 7 shows measured transfer characteristics of the PA. The PA performs a maximum output power of 15.6dBm and a power-added efficiency (PAE) of 10.1% (total Id=83mA) at 5.2GHz.

Figure 8 shows measured return-loss characteristics of the three-stage LNA. The bias condition is Vdd1=Vdd2=1.8V, Id (LNA total)=18mA. The input return-loss is 4.6dB and the output return-loss is 15.2dB at 5.2GHz. Figure 9 shows measured gain and NF characteristics of the three-stage LNA. The high gain of 20.6dB and the low NF of 3.3dB are obtained at 5.2GHz.

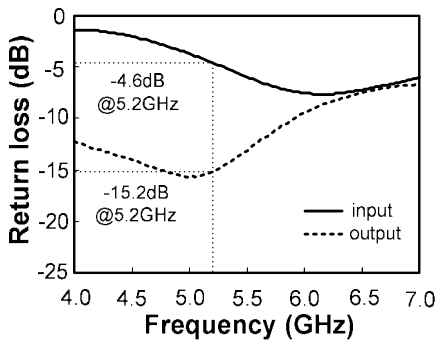

Fig. 8. Measured return-loss characteristics of the LNA.

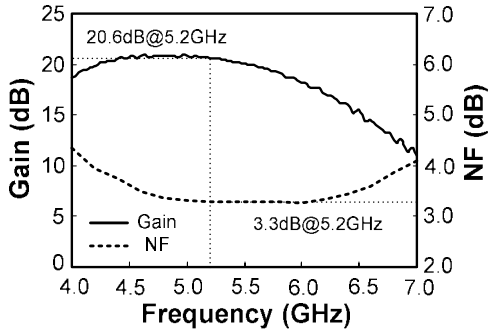

Fig. 9. Measured gain an NF characteristics of the LNA

Figure 10 shows measured frequency characteristics of the T/R switch between TX and ANT while terminating RX by 50Ω. The insertion loss is 0.83dB and the isolation is 22.8dB at 5.2GHz. The return-loss of TX and ANT are a high 23.2dB and 32.1dB, respectively. Figure 11 shows measured power-handling capability characteristics at 5.2GHz in the on-mode of the T/R switch. The bias condition is $V_{S/D}$=1V, V_{CTRL} =2.8V, $V_{\overline{CTRL}}$=0V. The high 1-dB gain compressed input power (IP_{1dB}) of 18.6dBm is obtained.

By using this IC, the RF characteristics of front-end is summarized in Table 1.

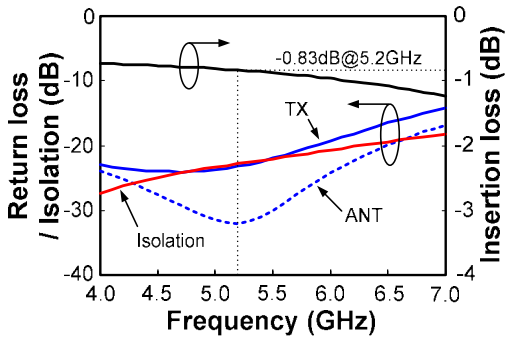

Fig. 10. Measured frequency characteristics of the T/R switch.

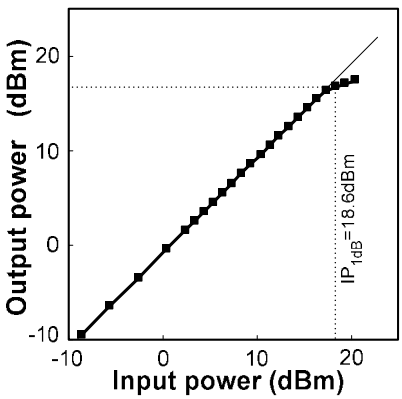

Fig.11. Measured power-handling capability characteristics of the T/R switch.

TABLE I
PERFORMANCE SUMMARY OF CMOS MMIC front-end

TX Chain	
Output Power Level	**14.8dBm**
Gain	**7.9dB**
Power Dissipation	**263mW**
RX Chain	
Noise Figure	**4.1dB**
Gain	**19.8dB**
Power Dissipation	**32mW**

V. CONCLUSION

A 5GHz-band CMOS MMIC front-end with fully monolithic internal matching circuits is developed in the 0.18μm CMOS process. The IC includes PA, LNA, and T/R switch. The high current spiral inductor successfully reduces the matching loss in transmitter chain. The IC performs 14.8dBm transmit power and 4.1dB receiver noise figure.

REFERENCES

[1] D. Su, M. Zargari, P. Yue, S/D. Su, M. Zargari, P. Yue, S. Rabii, D. Weber, B. Kaczynski, S. Mehta, K. Singh, S. Mendis, and B. Wooley, "A 5GHz CMOS Transceiver for IEEE 802.11a Wireless LAN," in *IEEE ISSCC Digest of Technical Papers*, pp. 92-93, Feb. 2002.

[2] M. Ono, N. Suematsu, S. Kubo, Y. Iyama, T. Takagi, and O. Ishida, "1.9-GHz/5.8-GHz-band on-chip matching Si-MMIC low noise amplifiers fabricated on high resistive Si substrate," in *IEEE RFIC-S Dig*., pp. 189-192, 1999.

[3] N. Suematsu and S. Shinjo, "CMOS/BiCMOS Power Amplifier Technology Trend in Japan," *IEEE GaAs IC Symp.Dig*., pp.107-110, 2001.

[4] M. Ono, N. Suematsu, S. Kubo, K. Nakajima, Y. Iyama, T. Takagi, and O. Ishida, "Si Substrate Resistivity Design for On-Chip Matching Circuit Based on Electro-Magnetic Simulation," *IEICE Trans. Electron*.,vol.E84-C(7), pp.923-930,July 2001.

[5] T. Ohnakado, A. Furukawa, M. Ono, E. Taniguchi, S. Yamakawa, K. Nishikawa, T. Murakami, Y. Hashizume, K. Sugahara, and T. Oomori, "A 1.4dB insertion-loss, 5GHz transmit/receive switch utilizing novel Depletion-layer-Extended Transistors (DETs) in 0.18μm CMOS process, " in Symp. *VLSI Tech. Dig. Tech. Papers*, pp. 162-163, 2002.

[6] T. Ohnakado, S. Yamakawa, T. Murakami, A. Furukawa, K. Nishikawa, E. Taniguchi, H. Ueda, M. Ono, J. Tomisawa, Y. Yoneda, Y. Hashizume, K. Sugahara, N. Suematsu, and T. Oomori, "A 0.8dB Insertion-Loss, 23dB Isolation, 17.4dBm Power-Handling, 5GHz Transmit/Receive CMOS Switch," in *IEEE RFIC-S Dig*., pp. 229-232, 2003.