

# Theoretical and Experimental Investigations on Nonlinear Capacitance and Loading Effects on Power PHEMT's Linearity

S. Forestier, T. Gasseling\*, P. Bouysse, D. Barataud\*, R. Quere, J.M. Nebus\*

IRCOM, CNRS, Université de Limoges, IUT GEII, 7 rue Jules Vallès, 19100 BRIVE, France

\*IRCOM, CNRS, Université de Limoges, 123 Av. Albert Thomas, 87060 LIMOGES, France

**Abstract**— This paper presents a theoretical and experimental analysis of the phase conversion phenomena in a power PHEMT transistor. Relationships between the linearity of the device and the intrinsic gate-source capacitance  $C_{GS}$ , gate-drain capacitance  $C_{GD}$ , transconductance  $G_M$  as well as the load impedance  $Z_L$ , are explained. A judicious choice of the transistor's operating conditions allows to reduce the phase conversion AM/PM. In the case of PHEMT devices, the behaviors of  $C_{GS}$ ,  $C_{GD}$ ,  $G_M$  elements and  $Z_L$  value induce internal compensation phenomena between the intrinsic non-linearities. These compensation mechanisms can be exploited to minimize the amplifier's phase conversion. The proposed approach is validated by comparisons between Load-Pull measurements at the frequency of 18 GHz and Harmonic Balance simulations. It reveals good accuracy for AM/PM predictions and shows the dependence of the phase conversion versus the load impedance and intrinsic non-linearities.

## I. INTRODUCTION

When designing an amplifier, in addition to the power performances, the linearity is a significant criterion for applications that require the amplification of variable envelope modulations. In order to reach a good linearity, the required objectives are power characteristics for which the gain and the phase conversions are both minimal whatever the variations of the input power. The intrinsic non-linearities of the transistor generate distortions which result in variations of the phase and the power gain [1]. These variations are at the origin of the degradation of the linearity criterion according to the input power level. The objective of this work is to analyze the phase conversion phenomena in PHEMT transistors.

The analysis focuses on the intrinsic non-linear phenomena which are at the origin of the phase conversion. In section II, a theoretical analysis, based on a simplified electrical model of the PHEMT device, points out the contribution of the intrinsic non-linearities to the phase conversion. It is shown that some non-linear effects can compensate themselves to reduce the phase conversion. Load-pull measurements have been performed in order to validate the theoretical study and are compared to non-linear simulation results in section III.

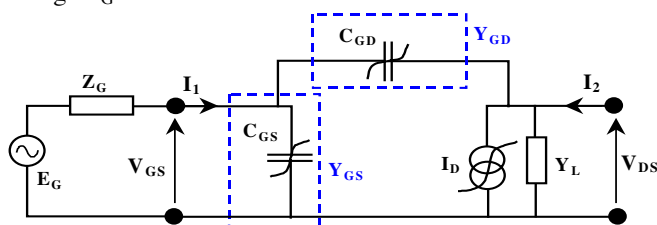
## II. THEORETICAL ANALYSIS OF PHASE CONVERSION

The electrical model used (Fig. 1) for the theoretical study is derived from the usual non-linear model of a FET transistor. Only the three main non-linear elements are kept. The model is

made of the non-linear gate-source and gate-drain admittances, respectively  $Y_{GS}$  and  $Y_{GD}$ , and of the drain current source  $I_D$ . Admittance  $Y_L$  represents the load admittance and impedance  $Z_G$  is the source impedance. For a normal operation of the amplifier, the effect of the gate-source diode and the gate-drain breakdown phenomena are considered as negligible.

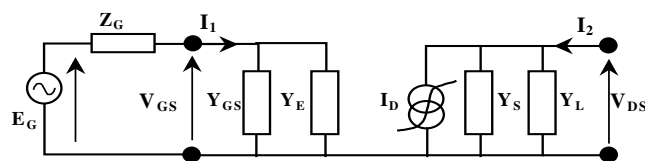
The drain current source  $I_D$  is considered, at first approximation, independent from the drain-source voltage  $V_{DS}$ , this corresponds to a zero drain conductance. The previous assumptions imply that the intrinsic dynamic load-line is limited to the saturation zone of the output current characteristics  $I(V)$ . In order to simplify calculations, the extrinsic passive elements of access are not taken into account explicitly but can be included in the elements  $Z_G$  and  $Y_L$  of figure 1. Series resistances  $R_{GS}$  and  $R_{GD}$ , usually associated with capacities  $C_{GS}$  and  $C_{GD}$  are ignored.

The application of Miller's theorem leads to the circuit presented on figure 2 by taking into account the input and output Miller admittances, respectively  $Y_E$  and  $Y_S$ . The phase conversion  $\Delta\phi$  is defined as being the variation of the phase  $\phi$  between the output drain-source voltage  $V_{DS}$  and the generator voltage  $E_G$ .



$Z_G$  : Source impedance  
 $Y_{GS}$  : Admittance associated with  $C_{GS}$   
 $Y_{GD}$  : Admittance associated with  $C_{GD}$   
 $Y_L$  : Load admittance

Fig.1 Simplified PHEMT model



$Y_E$  : Input Miller Admittance  
 $Y_S$  : Output Miller Admittance

Fig.2 Modified model (Miller's theorem)

The application of Miller's theorem leads to the expressions of the admittances  $Y_E$  and  $Y_S$  (eq. 1).

$$Y_E = Y_{GD} \left( \frac{G_M + Y_L}{Y_{GD} + Y_L} \right) \text{ and } Y_S = Y_{GD} \left( \frac{G_M - Y_L}{G_M - Y_{GD}} \right) \quad (1)$$

where  $G_M$  represents the drain transconductance associated to the drain current source  $I_D$ . The phase  $\varphi$  is calculated starting from equation (2):

$$\varphi = \text{Arg}^t \left( \frac{V_{DS}}{E_G} \right) = \text{Arg}^t \left( \frac{V_{DS}}{V_{GS}} \right) + \text{Arg}^t \left( \frac{V_{GS}}{E_G} \right) \quad (2)$$

$$\varphi = -\text{Arg}^t \left( \frac{G_M}{Y_S + Y_L} \right) - \text{Arg}^t \left( 1 + (Y_E + Y_{GS}) Z_G \right)$$

Hence :

$$\varphi = -\text{Arctg} \left[ \frac{\Im\{G_M / (Y_S + Y_L)\}}{\Re\{G_M / (Y_S + Y_L)\}} \right] - \text{Arctg} \left[ \frac{\Im \left\{ Z_G \cdot \left( Y_{GS} + Y_{GD} \left( \frac{G_M + Y_L}{Y_{GD} + Y_L} \right) \right) \right\}}{1 + \Re \left\{ Z_G \cdot \left( Y_{GS} + Y_{GD} \left( \frac{G_M + Y_L}{Y_{GD} + Y_L} \right) \right) \right\}} \right] \quad (3)$$

The following assumptions will allow us to reduce the previous expressions:

- the overall load admittance  $1/Z_{OPT}$  is the sum of the output admittances  $Y_L + Y_S$ . It is assumed to be only real and optimal for the output power matching of the transistor.
- the source impedance  $Z_G$  is real.
- The transconductance  $G_M$  is complex:  $G_M = |G_M| \angle \varphi_{Gm}$

Under these conditions, one shows that  $\varphi$  depends, at first order approximation, on the  $C_{GS}$ ,  $C_{GD}$  and  $G_M$  intrinsic elements and on the  $Z_G$  and  $Z_{OPT}$  extrinsic elements according to equation (4).

$$\varphi = -\varphi_{Gm} - \text{Arctg} \left\{ \frac{Z_G C_{GS} \omega}{+ Z_G C_{GD} \omega (1 + |G_M| Z_{OPT} \cdot \cos(\varphi_{Gm}))} \right\} \quad (4)$$

In order to perform a non-linear analysis, the elements  $C_{GS}$ ,  $C_{GD}$  and  $G_M$  of equation (4) must be replaced by their equivalent non-linearities  $C_{GS\_NL}(V_{GS1})$ ,  $C_{GD\_NL}(V_{GS1})$  and  $G_{M\_NL}(V_{GS1})$  at the fundamental frequency. These describing functions depend on the magnitude of the intrinsic voltage  $V_{GS1}$  at the fundamental frequency. The describing functions are determined with a harmonic balance simulation taking into account all the environment in which the non-linearities  $C_{GS}$ ,  $C_{GD}$  and  $G_M$  are placed.  $C_{GS\_NL}$  and  $C_{GD\_NL}$  functions are given with the computation of the imaginary part of  $Y_{GS}$  and  $Y_{GD}$  admittances at the fundamental frequency (eq. 5).

$$C_{GS\_NL}(V_{GS1}) = \frac{1}{\omega_o} \Im \left\{ \frac{I_{GS1}(V_{GS1})}{V_{GS1}} \right\} = \frac{1}{\omega_o} \Im \{ Y_{GS1}(V_{GS1}) \} \quad (5)$$

$$C_{GD\_NL}(V_{GS1}) = \frac{1}{\omega_o} \Im \left\{ \frac{I_{GD1}(V_{GS1})}{V_{GS1}} \right\} = \frac{1}{\omega_o} \Im \{ Y_{GD1}(V_{GS1}) \}$$

The function  $G_{M\_NL}$  is given by the computation of the fundamental current component  $I_{DS1}$  divided by the fundamental voltage component  $V_{GS1}$ . (eq.6)

$$G_{M\_NL}(V_{GS1}) = |G_{M\_NL}| e^{j\varphi_{GM\_NL}} = \frac{I_{DS1}(V_{GS1})}{V_{GS1}} \quad (6)$$

Hence, the phase  $\varphi$  depends on the voltage  $V_{GS1}$  (eq.7).

$$\varphi(V_{GS1}) = -\varphi_{GM\_NL} - \text{Arctg} \left\{ \frac{Z_G C_{GS\_NL} \omega}{+ Z_G C_{GD\_NL} \omega (1 + |G_{M\_NL}| Z_{OPT} \cdot \cos(\varphi_{GM\_NL}))} \right\} \quad (7)$$

The phase conversion  $\Delta\varphi$  is defined as the variation of  $\varphi(V_{GS1})$  compared to its small signal value. According to equation (7), the variations of  $C_{GS\_NL}$ ,  $C_{GD\_NL}$  and  $G_{M\_NL}$  can compensated themselves partially and lead to a minimal phase conversion  $\Delta\varphi$ . The capacities  $C_{GS}$  and  $C_{GD}$ , obtained by extraction along the intrinsic dynamic load-line on a  $8 \times 75 \mu\text{m}$  PHEMT transistor, are presented figure 3 [2,3].

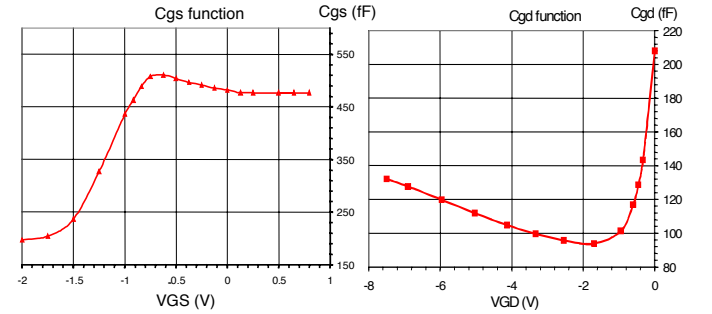


Fig. 3: Extracted capacities  $C_{GS}$  and  $C_{GD}$  versus bias voltages along the transistor output load-line.

The particularity of PHEMT devices is that the capacity  $C_{GS}$  decreases in the normal operating range of  $V_{GS}$ , in our case this appears for  $V_{GS}$  values greater than  $-0.7$  V. The direct consequence is the decreasing behavior of the non-linear function  $C_{GS\_NL}$  (Fig. 4) The describing functions  $C_{GS\_NL}$  and  $C_{GD\_NL}$ , simulated for different drain bias points, present opposite variations. Simulations have been made with a fixed gate source bias voltage at  $-0.5$  V and a load impedance  $Z_L = 11.6 - j2.2 \Omega$  at the frequency of 18 GHz.

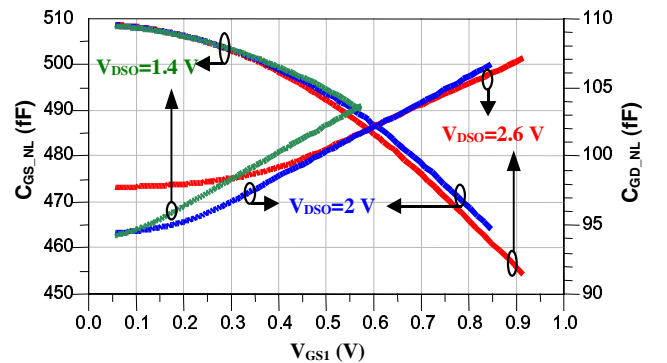


Fig. 4:  $C_{GS\_NL}$  and  $C_{GD\_NL}$  non-linearities with  $V_{GS0} = -0.5$  V and  $Z_L = 11.6 - j2.2 \Omega$

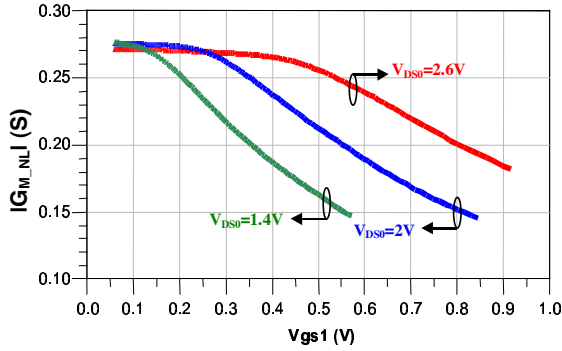


Fig. 5:  $|G_{M\_NL}|$  non-linearity

### III. EXPERIMENTAL RESULTS

The theoretical analysis has been validated on a  $0.15 \mu\text{m}$  gate length Power-PHEMT transistor with a  $8*75\mu\text{m}$  total gate width at the working frequency of 18 GHz.[4]

#### A. Influence of $C_{GS}$ capacity

The behavior of the  $C_{GS\_NL}$  non-linear function depends on the value of the gate bias point. The minimum phase conversion is obtained according to the equation (7) when the variation of  $C_{GS\_NL}$  compensates as well as possible, on the input power range, the variation of term " $C_{GD\_NL}(1+|G_{M\_NL}|Z_{OPT}\cos(\phi_{GM\_NL}))$ ".

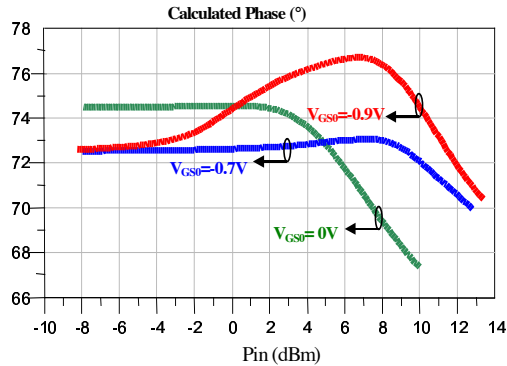


Fig. 6: Analytical calculation of  $\phi=f(V_{GS0})$

Experimentally, the dependence of  $\Delta\phi$  versus  $C_{GS}$  can be observed up to 2dB compression of the transistor's power gain by changing the gate bias point  $V_{GS0}$ . Three different values of  $V_{GS0}$  have been chosen, the load impedance  $Z_L=8.9+j.4.8\Omega$  and the drain bias point  $V_{DS0}=3\text{V}$  are kept fixed (Fig. 6 and Fig. 7). These results show that the phase conversion is minimum for  $V_{GS0} = -0.7\text{V}$ , this corresponds to a gate bias located in the region where  $C_{GS}$  capacity value (Fig. 3) is maximum and begins to decrease. Notice that the values of the phase  $\phi$  are different between analytical and experimental results, this is due to the fact that the analytical calculations are made with intrinsic voltages and it does not take into account the extrinsic passive elements. Nevertheless, the phase conversions  $\Delta\phi$  (variations of the phase  $\phi$ ) can be compared and the three analysis: analytical, experimental and HB simulations are coherent and give the same dependence of  $\Delta\phi$  with regards to the gate bias.

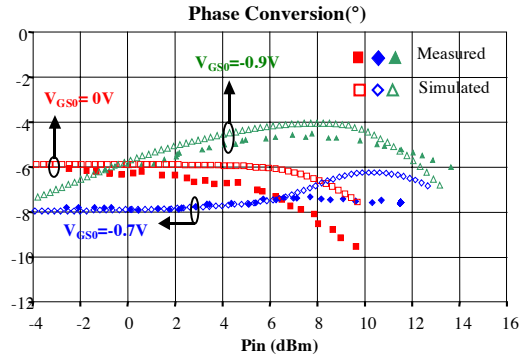


Fig. 7:  $\phi=f(V_{GS0})$  Load-pull measurements/ HB simulations

#### B. Influence of $C_{GD}$ capacity and $G_M$ transconductance

The influence of  $C_{GD\_NL}$  cannot be dissociated from that of the non-linear transconductance  $G_{M\_NL}$  since their contributions to the phase conversion are given by the term: " $C_{GD\_NL}(1+|G_{M\_NL}|Z_{OPT}\cos(\phi_{GM\_NL}))$ " (eq.7). Experimentally,  $C_{GD\_NL}$  and  $G_{M\_NL}$  vary according to the drain-source bias voltage  $V_{DS0}$ , without significant changes of  $C_{GS\_NL}$  and  $Z_{OPT}$ . The gate bias point  $V_{GS0}=-0.47\text{V}$  and the load impedance  $Z_L=11.5-j.2.3\Omega$  are kept unchanged. The phase conversion is then measured for various values of  $V_{DS0}$ . The curves (Fig. 8 and Fig. 9), plotted up to 3dB compression gain, show that the phase conversion decreases when  $V_{DS0}$  increases.

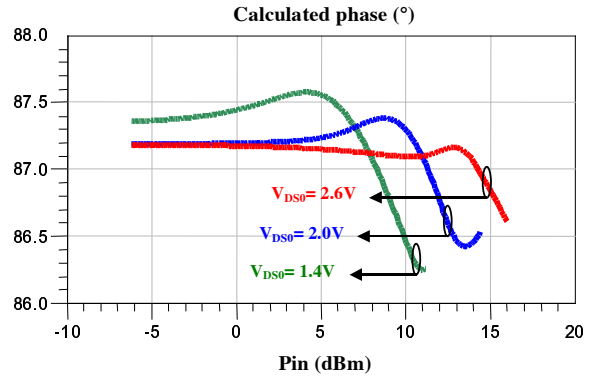


Fig. 8: Analytical calculation of  $\phi=f(V_{DS0})$

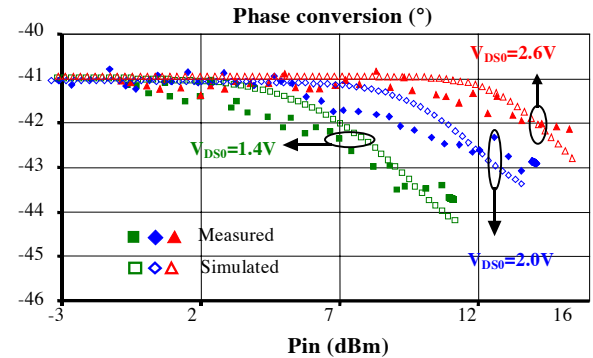


Fig. 9:  $\phi=f(V_{DS0})$  Load-pull measurements/ HB simulations

With a fixed load impedance, the growth in  $V_{DS0}$  value allows to increase the output power and thus to reach the same gain compression level for higher input powers. An increase in  $V_{DS0}$  makes it possible to move away the load cycle from the ohmic region of the  $I(V)$  characteristics and thus allows to reach the same power gain compression at a greater output power. The

influence of  $G_{M\_NL}$  is in this case most significant compared to that of  $C_{GD\_NL}$  and  $C_{GS\_NL}$  capacities.

### C. Influence of the load impedance $Z_L$

The phase conversion also depends on the load impedance  $Z_{OPT}$ . [5]  $Z_{OPT}$  represents the total equivalent impedance at the access of the intrinsic current source  $I_D$ . When the output circuit is properly tuned at the fundamental frequency, the imaginary part of  $Z_{OPT}$  is almost null. In this case, the intrinsic load line has a minimum area and  $Z_{OPT}$  is thus only a real impedance whose value controls the slope of the load line. Equation (7) shows that the value of  $Z_{OPT}$  controls the contribution of the  $C_{GD\_NL}$  non-linearity in the compensation phenomenon. Experimentally, a bias point ( $V_{GS0}=-0,47V$ ,  $V_{DS0}=3,2V$ ) is chosen in order to obtain the compensation phenomenon between  $C_{GS\_NL}$  and  $C_{GD\_NL}$ . Three different values of the module of the external load impedance  $|Z_L|$  are then used. The phase of the impedance  $Z_L$  is always chosen in order to minimize the load line area.

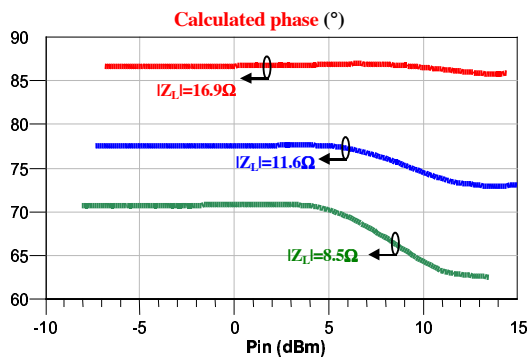


Fig. 10: Analytical calculation of  $\varphi=f(|Z_{OPT}|)$

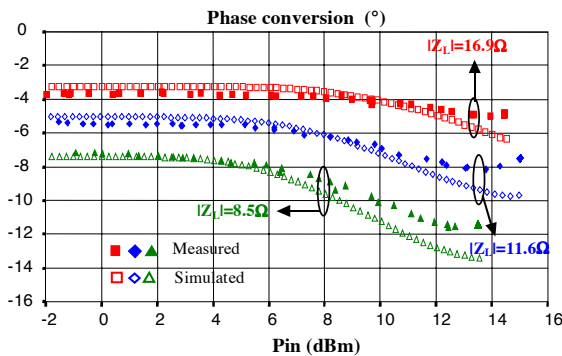


Fig. 11:  $\varphi=f(|Z_{OPT}|)$  Load-pull measurements/ HB simulations

The input power varies until the 4dB gain compression point is reached for each of the three values of  $|Z_L|$ . (Fig. 10 and Fig. 11) The most important phase conversion is obtained with the lowest value of  $|Z_L|$  ( $|Z_L|=8.5\Omega$ ). A minimum phase conversion is achieved with an impedance equal to  $|Z_L|=11.6\Omega$ . Simulations show that the variations of intrinsic impedance  $Z_{OPT}$  are similar to the variations of the extrinsic load impedance  $Z_L$ . Contrary to an usual operation of FET transistors, an increase in  $Z_{OPT}$  can improve the linearity of the PHEMT transistor. This is due to the particular behavior of the PHEMT gate-source capacity. Hence, the usual trade-off linearity/PAE according to the load impedance may not exist under particular operating conditions of the PHEMT device.

## IV. CONCLUSION

The simplified theoretical approach highlights the dependence of the phase conversion towards gate-source and gate-drain capacities and towards the load impedance. The results obtained on a  $8*75\mu m$  Power PHEMT device show first a good agreement between Load-Pull measurements and the large signal HB simulations and it also validate the non-linear model used. In addition, these results show the dependence of the phase conversion, by the means of the bias points, with regards to non-linearities due to the  $C_{GS}$  and  $C_{GD}$  capacities. A judicious choice of the bias point and of the load impedance allows to control the internal compensations phenomena in the PHEMT and make it possible to achieve a reduced phase conversion over a large input power range. Physical simulations [6] have shown that the particular form of the  $C_{GS}$  capacity is related to the gate recess. Other work [7] shows that the linearity of the amplifier is better in the case of a double recess compared to the simple recess. The study presented in this paper confirms these results and gives designing rules for the optimization of PHEMT amplifier's linearity.

## ACKNOWLEDGEMENTS

The authors would like to thank the CNES Toulouse for their contribution, especially L. Lapierre and A. Mallet and, P. Fellon of United Monolithic Semiconductors for all the help provided during this work.

## REFERENCES

- [1] T. Iwai, and al., "High Efficiency and High Linearity InGaP/GaAs HBT Power Amplifiers : Matching Techniques of Source and Load Impedance to Improve Phase Distorsion and Linearity ", IEEE Transactions on Electron Devices, vol. 45, n° 6, pp. 1196-1200, June 1998.
- [2] Staudinger and al., "An examination of Several Large Signal Capacitance Models to Predict GaAs HEMT Linear Power Amplifier Performance", , RAWCON'98 Proceedings, pp. 343-346, IEEE 98..
- [3] S. Forestier, and al., " A New Nonlinear Capacitance Model of Millimeter Wave Power PHEMT for Accurate AM/PM AM/PM Simulations", Microwave and Wireless Components Letters, pp.-, June 2003.
- [4] D. Barataud, and al., "Measurements and control of current/voltage waveforms of microwave transistors using an harmonic load-pull system for the optimum design of high efficiency power amplifiers", IEEE transactions on Instrumentation and Measurement, vol. 48, n° 4, pp. 835-842, August 99.
- [5] K. H. Ahn, and al., "Effects of Source and Load Impedance on the Intermodulation Products of GaAs FETs", MTT-Digest, vol. 1, pp. 469-472, 2000.
- [6] J. Hedoire, "Simulation hydrodynamique bidimensionnelle de transistors de type HEMT pseudomorphique. Analyse physique et optimisation pour l'amplification de puissance hyperfréquence", Thèse de doctorat. Université des Sciences et Technologies de Lille, n° d'ordre 2051 , 7 Juillet 1997.
- [7] C. Gaquière and al. , "Effects on the Linearity in Ka Band of Single or Double-Recessed PHEMT's", IEEE Microwave and Guided Wave Letters, Vol.10, N°.7, July 2000.