Characterisation of PHEMT intermodulation behaviour for highly linear MMIC power amplifier design

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In this paper the intermodulation distortion (IMD) behaviour of a 0.25 power PHEMT is investigated under several device operating conditions. An extensive experimental device characterisation, together with numerical simulations using suitable non-linear transistor models is carried out. Experimental data were compared with different transistor models in order to understand the effect of the various cell parameters on the device IMD₃ response. The data collected were applied in the design of a highly linear power amplifier family, covering different frequency ranges.

INTRODUCTION

Highly linear power amplifiers are key components for microwave radios using digital modulation schemes with high spectral efficiency. Improving trade-offs between linearity and power added efficiency (PAE) is extremely important to this kind of application so that several studies have been recently presented addressing this issue. We also proposed an approach for custom MMIC design where a trade-off between linearity and PAE was considered from the beginning of the design activity (Bignamini et al. (1)). For this purpose a successful design will necessarily be based on a suitable non linear model, able to predict both gain and IMD₃ distortion with a certain degree of precision, or on a sufficiently large amount of experimental data.

In this paper we investigate the non-linear behaviour of a 0.25 power PHEMT as a function of many operational parameters, as frequency, source and load impedance. The data collected are analysed in many different frameworks, first adopting extremely simplified models, then using more accurate models, in order to understand the origin of the observed behaviour.

EXPERIMENTAL SET UP

A block diagram of the experimental set up, is shown in fig. 1. Two RF signals are independently generated and amplified before being combined at the input of DUT. The PHEMT is biased by means of bias-tees (omitted in the picture). The source and load impedance are tuned by means of two passive tuners and measured with a HP8510 network analyzer. In order to extend the

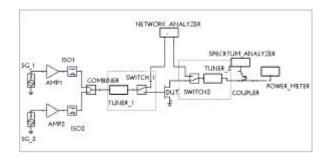


Figure 1: Experimental set up

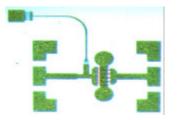


Figure 2: Test device with the pre-matching network

tunability range of input cell terminations to the low resistance region, a pre-matching network was designed (see fig. 2).

The input and output network are connected to the DUT by means of two switches. A 10 dB directional coupler at the output allows the simultaneous measurement of output power and IMD_3 distortion.

RESULTS

In this paper we focus our attention on a set of measurements performed on a 600 μ m PHEMT @ 13 GHz, biased with V_d = 6.5 V and I_d = 60 mA. In fig. 3 are shown IMD measurements performed with the load impedance fixed at its optimum value, previously determined with a 50 Ohm input termination (Z_{out}=(27+j32 Ω), for different values of the resistive part of the source impedance.

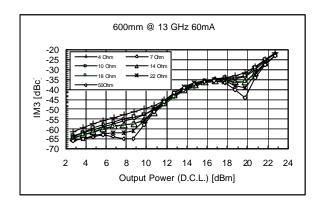


Figure 3: IMD₃ distortion as a function of output power for different source impedances

The reactive part was also kept constant and equal to zero. Although at a very low power level IMD_3 is unaffected by the source termination, increasing the power the presence of two "spots" in IMD_3 distortion can be observed.

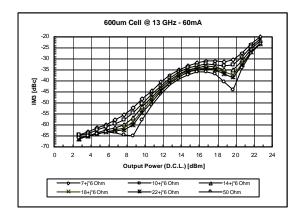


Figure 4: IMD₃ as a function of output power for different source impedances with a non zero reactive component.

The dependence of IMD₃ by source impedance disappears in a moderately high power level range.

In figure 4 are shown measurements performed introducing a reactive part in the source impedance. The behaviour is similar, but in this case changes in IMD_3 distortion with the input termination can be observed in the whole high power range.

DISCUSSION

To understand the origin of the observed behaviour, and in particular the parameters that influence the IMD_3 spots, we analysed the experimental data in different frameworks. The simplest model we considered is the widely accepted equivalent circuit shown in fig. 6. We adopted the following strong simplifications:

- The dependence of all parameters by V_d was not considered.
- The only non linear components we considered were the gate-source capacitance (C_{gs}) and the drain current generator (G_m) , as non-linear function of $V_{gs.}$

To extract the model parameters we proceeded as follows. We measured the cell S parameters at a moderately low frequency (900 MHz) as a function of the gate bias voltage V_{gs} . In this frequency range the input and output parasitic capacitances can be neglected. From the S parameters we calculated the Z parameters. Then we evaluated the Z parameters of the intrinsic model de-embedding the parasitic impedance at the cell terminals:

$$\mathbf{Z'} = \mathbf{Z} - \mathbf{Z}_{\boldsymbol{e}} \tag{1}$$

with

$$\mathbf{Z}_{e} = \begin{bmatrix} Z_{s} + Z_{g} & Z_{s} \\ Z_{s} & Z_{s} + Z_{d} \end{bmatrix}$$
(2)

The value of Z_g , Z_s , and Z_d , were given by the foundry. From Z' we calculated the intrinsic admittance matrix Y' and then the required parameters:

$$C_{gd} = -\frac{\operatorname{Im}(Y'_{12})}{W}$$
(3)

$$R_{i} = \operatorname{Re}\left(\frac{1}{Y_{11}' - j \mathbf{w} C_{gd}}\right)$$
(4)

$$C_{gs} = -\frac{1}{w \operatorname{Im}\left(\frac{1}{Y_{11}' - jwC_{gd}}\right)}$$
(5)

$$R_{ds} = \frac{1}{\operatorname{Re}(Y'_{22} - j \mathbf{w} C_{gd})}$$
(6)

$$C_{ds} = \frac{\mathrm{Im}(Y_{22}' - j\mathbf{w}C_{gd})}{\mathbf{w}}$$
(7)

$$G_m = \left| \left(Y'_{21} + j \mathbf{w} C_{gd} \right) \left(1 + j \mathbf{w} C_{gs} R_i \right) \right|$$
(8)

$$\boldsymbol{t} = -\frac{\angle \left[\left(Y_{21}' + j \boldsymbol{w} \boldsymbol{C}_{gd} \right) \left(1 + j \boldsymbol{w} \boldsymbol{C}_{gs} \boldsymbol{R}_{i} \right) \right]}{\boldsymbol{w}}$$
(9)

As a further approximation, C_{gs} and G_{h} behaviour was approximated in a small region around the bias point with a 5th order polynomial function.

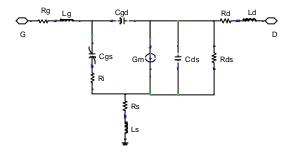


Figure 5: PHEMT equivalent circuit

In order to separately analyse the C_{gs} and G_m contribution to IMD₃ distortion, we first simulated the circuit with a non-linear C_{gs} and a linear G_n . Then we simulated a circuit with a linear C_{gs} and a non-linear G_m . As final step we introduced both C_{gs} and G_n non-linearities. For each of this case was performed a source pull. Some of the results obtained are shown in fig. 6 and 7 and can be summarised as follows:

- The high power spot can be easily reproduced simply considering the G_n non-linearities up to the 5th order and is the effect of the 180 degree out of phase combination of IMD₃ coming from

the 3^{rd} order term with the one due to the 5^{th} order term.

- Even if the framework is extremely simplified, the model predicts a remarkable influence of source termination on IMD₃. This effect, present in our measurements (fig. 3 and 4), is widely discussed in literature (J. A. Garcia et al. (2), Kwang-Ho Ahn et al. (3)).
- The introduction of non-linearities in the C_{gs} decrease IMD₃ over the entire power range considered (fig. 6). The Intermodulation distortion decrease depends on the phase difference between the IMD₃ due to C_{gs} and the one due to G_m .

The low power spot cannot be explained in this simplified scheme because the phase difference of G_n and C_{gs} non-linearities is almost independent by the power level. For this reason the two non-linearities will combine always in the same way, increasing or decreasing the overall IMD₃. distortion, having the same effect over the whole power range.

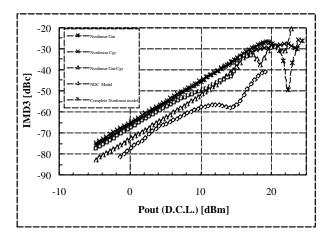


Figure 6: Comparison of different simulations performed with various non linear models with $Z_{in}=22$ W and $Z_{out}=(27+j32)$ W

To complete the analysis we compared our experimental data with more accurate models. A spot-like behaviour can be observed using the same equivalent circuit of fig. 5, but introducing other non linear elements (as R_{ds} and C_{gd}). A better agreement can be obtained using a more sophisticated model taking into account other relevants effect (V_d dependence, memory effects, etc.). For example a low power spot can be observed in a wide range of load and source impedance with the Nonlinear Discrete Convolution (NDC) Model discussed in Filicori

et al. (4) and Costantini et al. (5). This model takes into account the short time memory effect of the device and predicts its non linear behaviour on the basis of the device small signal behaviour.

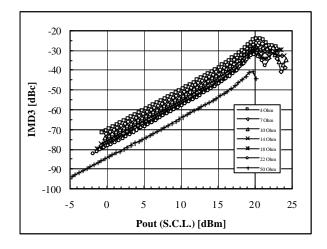


Figure 7: Source pull with the simplified nonlinear model

However, the complexity and the generality of the NDC approach doesn't allow an immediate interpretation of the spot presence in terms of the device parameters.

CONCLUSIONS

As a step of a complete development procedure set up to design highly linear power amplifiers, a characterisation of the third order intermodulation distortion behaviour of a 0.25 power PHEMT technology was investigated. An extensive experimental device characterisation, together with several numerical simulations, were performed. Starting from very simplified models we discussed separately the effects of the non linear gate-source capacitance and the non linear drain current generator, in order to understand the observed device behaviour. Some of the main observed features can be easily explained even in a very simplified framework. The accurate prediction of the device behaviour and other peculiar effects, as the low power spot, can be addressed only using more complete non-linear models. An example can be the Non-Linear Discrete Convolution Model described in ref. (4), (5).

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