A 6-18 GHz 5-Bit Phase Shifter MMIC Using Series/Parallel LC Circuit

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***Abstract* — A high performance 6-18 GHz 5-bit reflection type phase shifter MMIC is presented. It employs a novel ultra-broad-band circuit design technique utilizing a series/parallel LC circuit for an 180° phase shift over all frequencies. The fabricated phase shifter MMIC with SPDT switch suitable for T/R modules has demonstrated a typical insertion loss of 9.4 dB +/- 1.4 dB, a maximum RMS amplitude error of 0.33 dB and a maximum RMS phase error of 7° over entire operating bandwidths.**

I. Introduction

Broad-band phase shifters have been required in wideband phased array systems for electronic beam steering. A reflection type phase shifter is able to operate in a relatively wide frequency range over other circuit designs [1]-[3]. However, the chip size is tending to be large mainly due to 3-dB hybrid couplers used in it. To minimizing the size, the high-pass/low-pass switched structure was applied to broad-band phase shifter circuit designs at the expense of the operating bandwidths [4][5]. Another approach to broad-band phase shift characteristics is to employ the analog phase shift circuit design techniques [6][7]. Though the size of the analog phase shifter is small, it cannot achieve a flat phase shift versus frequency over the control voltage.

This paper describes a broad-band reflection type 5-bit phase shifter with the accomplishment of a high performance and a small size. A circuit for each bit of the phase shifter is composed of a broad-band 3-dB Lange coupler and a pair of reflective terminating circuits. With a novel ultra-broad-band circuit design technique utilizing series/parallel LC circuit, an exact phase shift of 180° can be achieved theoretically for all frequencies [8]. The 6-18GHz 5-bit phase shifter MMIC with single pole double throw (SPDT) switch has been designed and fabricated. The phase shifter MMIC with SPDT switch has achieved a typical insertion loss of 9.4 dB +/- 1.4 dB, a maximum RMS amplitude error of 0.33 dB, and a maximum RMS phase error of 7° over the operating frequency band. This excellent performance is suitable for wideband phased array applications.

II. Design

The schematic diagram of the proposed 5-bit phase shifter MMIC with SPDT switch suitable for transmit/receive (T/R) modules is illustrated in Figure 1. The MMIC chip is composed of a phase shifter section and a series-shunt FET SPDT switch section. The phase shift circuits design of the 5-bit phase shifter is based on the reflection type topology consisting of a 3-dB Lange coupler and a pair of reflective terminating circuits with switching FETs. The fabricated 5-bit phase shifter MMIC with SPDT switch is shown in Figure 2. The IC has been fabricated by using 0.5 μm p-HEMT technology. The total chip size is 4.27 mm x 3.17 mm including the 5-bit phase shifter section of 3.47 mm x 3.17 mm.

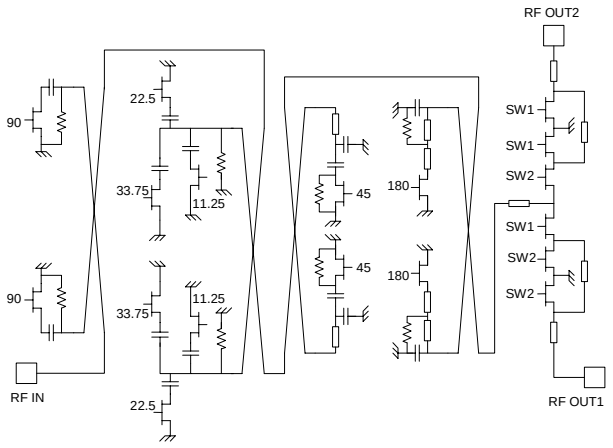

Figure 1. Schematic diagram of the proposed 5-bit phase shifter MMIC with SPDT switch.

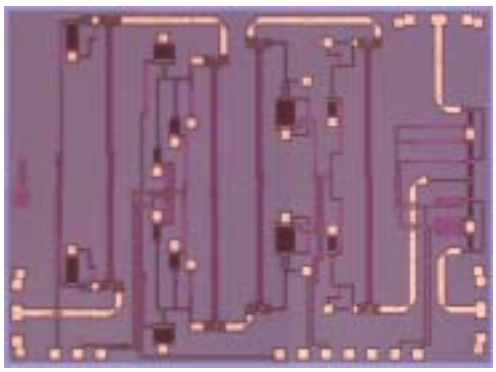

Figure 2. Photograph of the fabricated 5-bit phase shifter MMIC with SPDT switch.

The schematic diagram of the novel 180° reflective terminating circuit is shown in Figure 3. It consists of only a few circuit elements, an inductor L, a capacitor C and an FET. The FET is used as a switching element.

Figure 4 shows equivalent circuits of series and parallel LC states of the 180° reflective terminating circuit. R_{on} and C_{off} are the on-state resistance and the off-state capacitance of FET, respectively. When the FET turns on, the circuit corresponds to parallel LC circuit consisting of L and C shown in Figure 4 (a) by neglecting R_{on}. When the FET is pinched off, the circuit can be simplified to a series LC circuit consisting of L and C_{off} shown in Figure 4 (b) if admittance of C is small enough to be neglected. Therefore, the circuit shown in Figure 3 can be regarded as a switching series/parallel LC circuit. When the resonant frequency of the series and the parallel LC circuits is set to be ω_0, circuit elements of L, C and C_{off} are determined uniquely given as follows

$$L = \frac{Z_0}{\omega_0} \tag{1}$$

$$C = C_{off} = \frac{1}{\omega_0 Z_0} \tag{2}$$

Z_0 is the impedance of the port of 3-dB Lange coupler. In the above condition, a phase difference between reflection phase in the series LC state and that in the parallel LC state is exactly 180° for all frequencies theoretically. The theory was described in reference [8] in more detail. However, the return loss in the parallel LC state particularly appears at ω_0 by the non-zero R_{on}. In practical design, ω_0 has to be optimally determined higher than the operating frequency band. Also, a resistor is incorporated between source and drain terminals of FET to equalize the magnitude of reflection coefficient in series and parallel LC states. That resistor has a negligible effect on phase difference and impedance of the circuit.

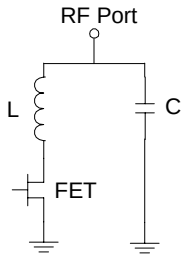

Figure 3. Schematic diagram of the novel 180° reflective terminating circuit.

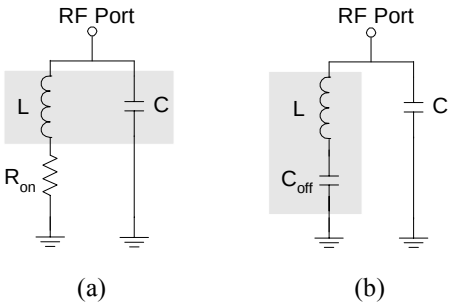

Figure 4. Equivalent circuits of the novel 180° reflective terminating circuit. (a) Parallel LC State. (b) Series LC State.

The 90°, 45° and 22.5°/11.25° bit reflective terminating circuits are based on digitally controlled capacitive circuit design. These circuits are composed of capacitors and switching FETs. The total capacitances of the reflective terminating circuit are set to be C_a and C_b in the phase shift state and the phase reference state, respectively. To obtain broad-band phase shift characteristics, C_a and C_b are determined as follows

$$C_a = \frac{1}{\omega_c Z_0} e^{\frac{\Delta\theta}{2}}, \quad C_b = \frac{1}{\omega_c Z_0} e^{-\frac{\Delta\theta}{2}} \tag{3}$$

ω_c is the center frequency of the operating frequency band. $\Delta\theta$ is the desirable phase shift.

The 11.25° and 22.5° bit reflective terminating circuit are combined into one circuit which has four phase shift states. This circuit design can achieve size reduction and low loss characteristics compared with a bit circuit fabricated separately. To realize 33.75° phase shift, aseries combination of a capacitor and a FET is added shown in Figure 1.

III. MEASUREMENT RESULTS

The measured results of the fabricated 5-bit phase shifter MMIC with SPDT switch in all 32 phase states are shown in Figure 5-7 with a control voltage of -3.0 V. The measured input and output return loss were 8.8 dB and 11.8 dB at the worst case respectively in the 6 to 18 GHz band. The typical insertion loss was 9.4 dB +/- 1.4 dB over the same frequency range. A maximum RMS phase error was 7^{o} plotted in Figure 8, and a maximum RMS amplitude error was 0.33 dB plotted in Figure 9 in the operating band frequency. In particularly, the chip also showed very good performances over the typical midband. At 10 GHz, the insertion loss was 9 dB +/- 0.16 dB, and the RMS phase error was 2.6^{o}. The 5-bit phase shifter with SPDT switch still keeps effective performance over the designed frequency band. The RMS phase error over high frequency band was mainly due to phase shift error of the 180^{o} bit circuit. Some improvements of the performance of the 180^{o} bit circuit are possible. The measured performance is summarized in Table 1.

The measurements of the MMIC with a solo SPDT switch are shown in Figure 10. The measured insertion loss was less than 1.48 dB over the 6 to 18 GHz band, and the isolation was more than 30.9 dB in the operating bandwidths.

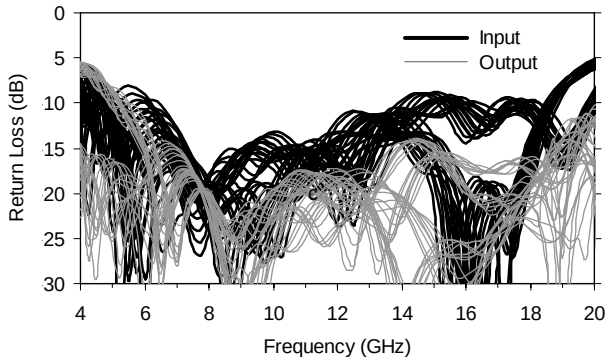

Figure 5. Measured input and output return loss in all 32 phase states.

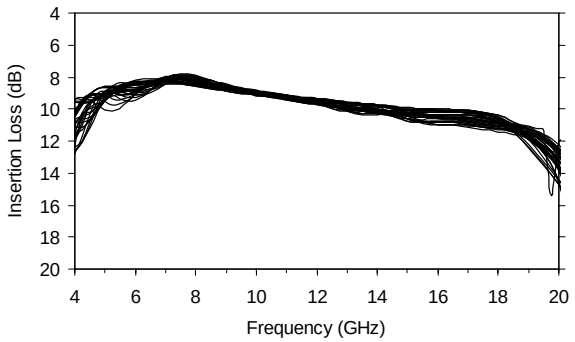

Figure 6. Measured insertion loss in all 32 phase states.

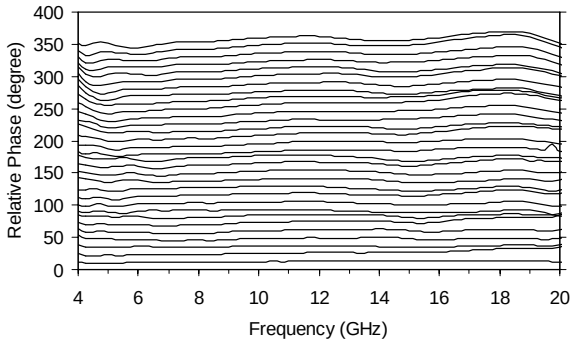

Figure 7. Measured phase shift in all 32 phase states.

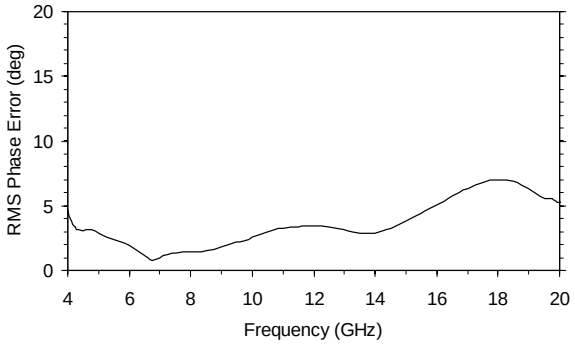

Figure 8. Measured RMS phase error.

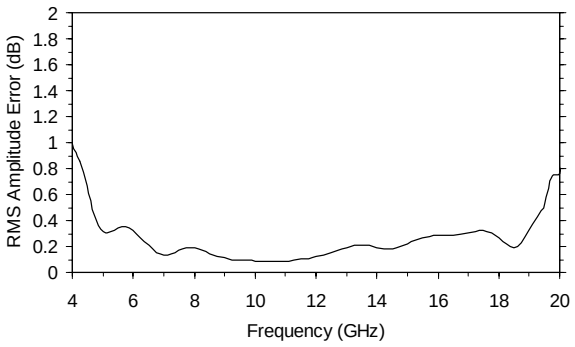

Figure 9. Measured RMS amplitude error.

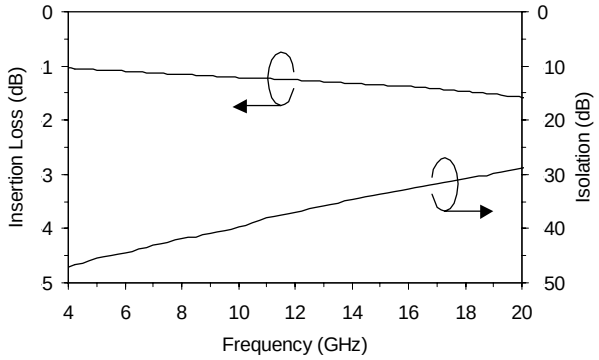

Figure 10. Measured insertion loss and isolation of the SPDT switch.

Table 1. Summary of the measured performance of the 5-bit phase shifter MMIC with SPDT switch over the 6 to 18 GHz.

Parameter	Value
Min. Input Return Loss	8.8 dB
Average Input Return Loss	12.2 dB
Min. Output Return Loss	11.8 dB
Average Ouput Return Loss	16.9 dB
Average Insertion Loss	9.4 dB +/- 1.4 dB
Max. RMS Phase Error	7^o
Average RMS Phase Error	3.3^o
Max. RMS Amplitude Error	0.33 dB
Average RMS Amplitude Error	0.19 dB

IV. Conclusion

A broad-band 5-bit reflection type phase shifter was developed. The phase shifter employs a novel ultra broad-band circuit design technique utilizing a series/parallel LC circuit for a 180^o phase shift over all frequencies. The fabricated phase shifter MMIC with SPDT switch suitable for T/R modules has successfully demonstrated a typical insertion loss of 9.4 dB +/- 1.4 dB, a maximum RMS amplitude error of 0.33 dB and a maximum RMS phase error of 7^o over the 6 to 18 GHz band. That excellent broad-band performance is suitable for wideband phased array applications.

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