A GaAs MMIC CHIP-SET FOR 10 to 15GHz RADIO-LINKS APPLICATIONS

P. Quentin[1], A. Gallien[1], F. Rasà[2], B. Gabbrielli[2]

[1]United Monolithic Semiconductors, RD128, BP46, 91401 ORSAY, Cedex, France
Tel. 33-1-6933-0587 / Fax. 33-1-6933-0552 / e.mail pierre.quentin@ums-gaas.com
[2]Alcatel Italia, str. provinciale per Monza, 33, 20049 Concorezzo (MI), Italy
Tel. 39-039-686-5664 / Fax. 39-039-686-5600 / e.mail francesco.rasa@netit.alcatel.it

Abstract - This paper describes the development of a GaAs MMIC chip-set for Ku-band radio-links transmitter. This chip-set includes two circuits, a times-two multiplier 5-7.5GHz to 10-15GHz, and a single side band up-converter. The development and the results of these circuits are analysed.
The times-two multiplier is based on a specific balanced configuration leading to a very high level of input frequency suppression at the output (typically 50dBc) on a 2.7mm² chip. The mixer circuit is a broadband build-in single side band mixer of 10mm², with typically 30dBc image suppression.

I. INTRODUCTION

The communication market is booming. Ku-band is part of this game, and more and more the price pressure leads to re-design of the radios, including architecture, in order to use as much MMICs as possible leading to lower size, lower price and higher degree of manufacturability.

The previous designs were widely based on discrete components leading to large board size, assembly and tuning efforts. The MMICs offer broadband capabilities and help to reduce the tuning and assembly cost. For a specific transmitter radio in Ku band, we developed a broadband multiplier circuit with high level of suppression of the input frequency, and a broadband single side band mixer with high linearity capabilities. These two circuits will be used for the up-conversion block in the SDH2G (Second Generation of Synchronous Digital Hierarchy) family of Alcatel high capacitance transmission systems. The designs are based on the standard UMS HP07 design book.

II. TIMES TWO MULTIPLIER

This circuit is to be used for the local oscillator chain of a typical Ku band radio. The target was to include on chip as much functionality as possible, and being able to drive directly the mixer chip. For this, the circuit includes a multiplier in balanced configuration, a stop band filter and a three-stage amplifier. The layout of this circuit is shown in figure 1.

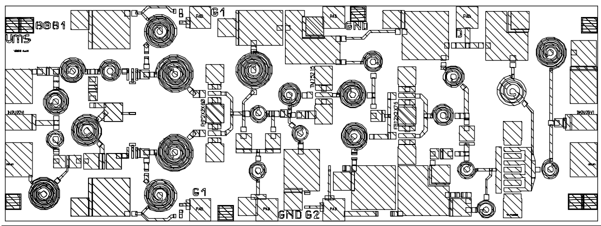

Fig. 1 : Layout of the times two multiplier.

A. Balanced multiplier

The specific topology used aims to suppress the input frequency leakage at the output thanks to a balanced configuration. The two multipliers, strictly identical, are fed via a phase shifter network with signals out of phase (+90° / -90°). This network is realised with lump elements to reduce the chip size. The multiplier cell is based on a transistor biased at pinch-off. The output is combined in phase at the output of the multiplier. This in-phase combiner is realised very simply by a direct connection of the two drains of the multiplier device. Doing so, the second harmonics out from the multipliers are in phase, and the fundamental signals are in phase opposition, and then cancelled.

B. Stop band filter

Furthermore, we include on chip a specific stop band filter to suppress even more the input frequency.

This filter is realised with lump elements in order to save space.

C. Amplifier

The output signal from the multiplier is then amplified to such a level that it will be possible to drive directly the mixer. This amplifier is designed on a narrow band basis in order to avoid as much as possible the leakage of the other spurious frequencies such as the 3*Fin and 4*Fin. The output power has to be higher than +16dBm, working in saturated mode to limit the power variations in temperature. This is required to be able to drive directly the single side band mixer without any filter due to the very good spurious performances and without any other buffer amplifier. Furthermore, the process use for the two circuits is the same, leading to the possibility of a single chip multifunction realisation for very high volume requirements.

D. Multiplier characterisations

The characterisation of the times two multiplier has been performed in a specific test-jig. The obtained results are given in figure 2 for the spurious response. The input frequency suppression reaches up to 50dBc in the 10 to 14GHz, and still exhibits more than 40dBc in the full frequency band, as related to the output frequency of the times two multiplier.

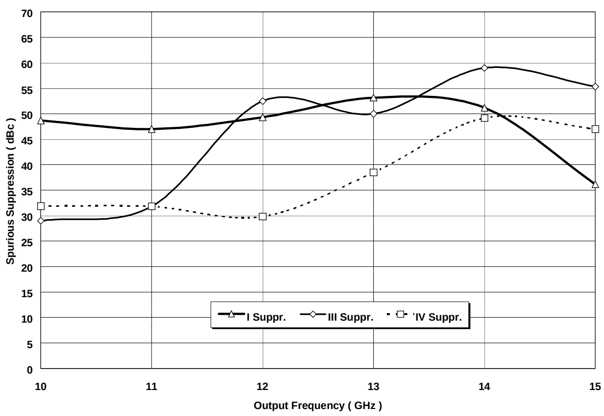

Fig. 2 : Typical Spurious suppression
(dBc @ output).

The 3*Fin and 4*Fin spurious frequencies are better than 30dBc across the full frequency band.

The typical measured conversion gain is given in figure 3. This conversion gain is in the range of –0.5dB ±1.5dB for an input power of +17dBm, so the output power reaches 17dBm in order to be able to drive the mixer. The conversion gain ripple in-band comes from the buffer amplifier. This was corrected on a re-designed circuit that should be available and characterised for the oral presentation.

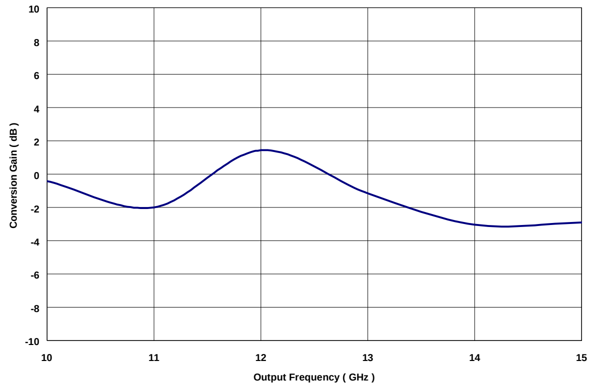

Fig. 3 : Typical conversion gain
(dB @ P_in=17dBm).

III. MIXER

The mixer used as an up-converter is one of the most critical circuits in a communication radio. It is mandatory, for such circuit, to avoid as much as possible the spurious generation, and at the same time to keep linearity at high level.

A. Design

The chip that was designed is based on the combination of four mixers in order to provide a single side mode. The layout of this circuit is given in figure 4.

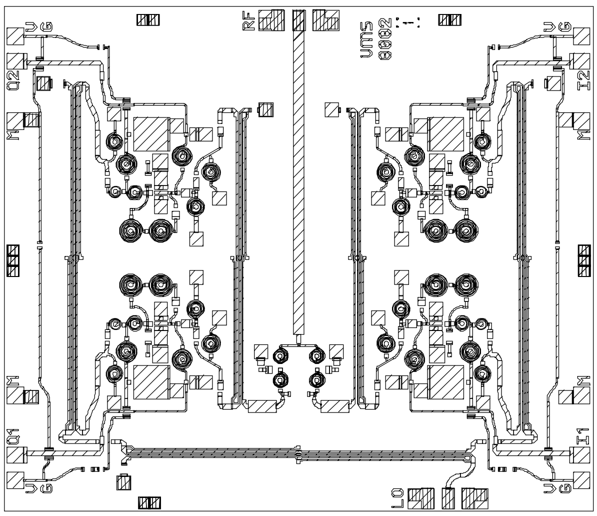

Fig. 4 : Layout of the Ku band mixer.

That means that we had to balance two mixer cells in phase opposition to suppress the local oscillator, and then balance two of these mixer pair in quadrature to suppress the image. The intermediate frequency has to be fed on four accesses, in quadrature from one to the other. A specific external intermediate frequency power divider has to be used. For chip size reasons, it was not possible to include this combiner on chip. In order to reach broadband performances, we have chosen to base the design on combination of Lange couplers. The mixer cell itself is based on cold FET for linearity, using a specific feedback topology, to improve the LO/RF isolation of the single mixer cell.

B. Mixer characterisations

The mixer characterisation has been performed in a specific test-jig, including a proprietary external IF divider to feed the four quadrature IF signals. The result shown here includes these divider and package effects.

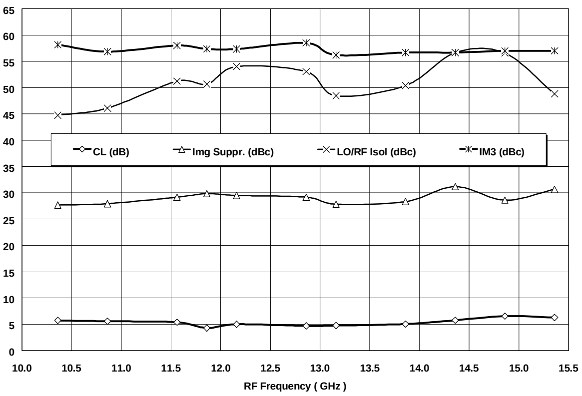

Fig. 5 : Typical mixer measurements
in LSB configuration.

The obtained results are summarised in figure 5 for Lower Side Band operation mode, and in figure 6 for the Upper Side Band mode. The conversion losses are in the range of 5dB for a local oscillator power of +17dBm. The IF frequency is fixed to 140MHz, for an input power of +5dBm at the input of the IF divider. In the same conditions, the image suppression ranges from 27dBc to 30dBc, and the LO to RF isolation is better than 45dBc. The measured IM3 is better than 55dBc, also in the full frequency band.

These results, as shown on the two graphs, are very consistent in the two modes, LSB and USB.

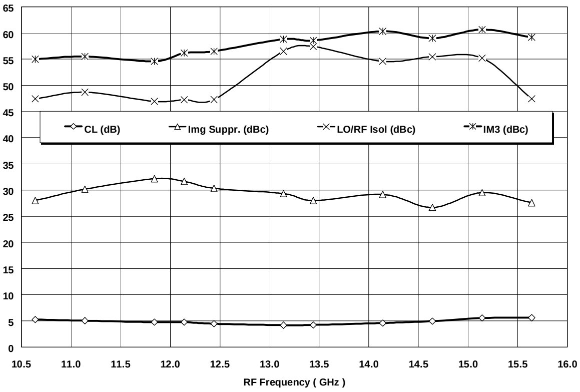

Fig. 6 : Typical mixer measurements
in USB configuration.

IV. CONCLUSIONS

This work present ready to produce high performances MMICs for radios in Ku band, introducing a compact balanced multiplier configuration avoiding the use of external filter between this circuit and the mixer. The mixer itself, providing internal cancellation of the image frequency signal and of the local oscillator leakage, lead to a very easy implementation of a transmitter for communication radios. These circuits are realised on the proven UMS MESFET process (HP07), willing to offer low cost MMIC solutions up to Ku frequency band.

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The authors would like also to pay tribute to J. Primon, who initiated this project, and unfortunately left us last year.

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