

Flip-chip for space applications : Bonding reliability, DC and RF results.

Sébastien George, Claude Drevon, Jean-Louis Cazaux

ALCATEL SPACE INDUSTRIES - BP1187 - 31037 TOULOUSE Cedex1 - France

sebastien.george@space.alcatel.fr

Abstract - This paper presents a study of flip-chip bonding for space applications. DC and mechanical test vehicles have demonstrated the reliability of the flip-chip gold-gold thermocompression bonding up to 500 thermal cycles. RF test vehicles have proved the compatibility of both coplanar and microstrip on-the-shelves MMICs with the flip-chip bonding up to 35 GHz.

I. INTRODUCTION

The flip-chip bonding technology is now adopted for consumer products fabrication. Cellular phones, watches, automotive and telecommunication electronics make use of with flip-chipped ICs. This technology provides higher packaging density, lower interconnect parasitics, lower fabrication costs and becomes necessary with the increasing frequency of telecommunication systems. It will be the next evolution in space application as well.

II. BUMPS AND FLIP-CHIP ASSEMBLY

The re-use of already developed MMICs for flip-chip mounting together with a wide range of substrate types (like thin film alumina, AlN, MCM-C...) leads us to choose the gold stud bumps and the gold-gold thermocompression bonding. The long term goal is to supply MMICs with gold bumps directly grown on-chips at the GaAs foundry. That will fulfill large volume requirements.

The available MMICs for that study were a thinned (microstrip) daisy-chain generic chip and microstrip and coplanar MMIC amplifiers in Ku and Ka bands.

The daisy-chain vehicle allows us to verify the compatibility of gold stud bumps with GaAs dice and substrate materials. Our low level applications use alumina-type substrates (mono-layer thin films or multi-layer HTCC) and the more advanced AlN substrates for power applications. Then, the daisy-

chain test vehicle has been both implemented on these two types of substrates.

The amplifiers are bonded on alumina only.

Stud bumps shear strength is above 30-35 g. for single and double stud bumps on the sputtered Nickel Gold thin film. Die shear tests have been performed to check the validity of the flip-chip bonding profile (295°C / 30 g. per bumps) on alumina substrate (Al₂O₃) with thermal cycling aging between -55°C and +125°C. The results per bumps are summarized in TABLE 1.

Table 1 : EVOLUTION OF DIE SHEAR STRENGTH WITH TEMP. CYCLING (Al₂O₃ SUBSTRATE)

	Init.	100 c.	200 c.	500 c.
Mean	36.1 g	37.9 g	34.8 g	35.3 g
std dev.	3.4 g	6.6 g	2.6 g	2.6 g

This has to be compared with a minimum of 5 g. per bump given by MIL STD 883-Method 2011 for flip-chip bonding.

III. DAISY-CHAIN

A. Test Vehicle design

The size of the daisy-chains GaAs chip is about 5 x 5 mm² and is representative of the most of our MMICs.

The daisy-chain MMIC and the host substrate permit two kinds of measurements : single bump resistance extraction and a 12 bumps daisy-chain resistance extraction. The measurements are performed in 4 wires configuration with a GPIB test bench where any of the 2 bumps bridges can be reached for failure localization. All the test bench is functioning, with about 0,05 mΩ resolution.

B. Results

The different Test Vehicles at initial time show a 1 mΩ average contact resistance per bump. This bump contact resistance value does not permit to

visualize resistance evolution on daisy-chains except the open-type failure.

The evolution of the contact resistance of each test vehicle type is summarized in TABLE 2 for Al_2O_3 , TABLE 3 for AIN without underfill and TABLE 4 for AIN with underfill.

The tables 2 to 4 have the same structure. The first three lines deal with the daisy-chain resistance measurements. We do not observe any variation on the resistance value, except for the open-type failure of the AIN substrates without underfill. The failure line is the number of open bump versus the total number of bumps. The last two lines deal with the single bump measurements.

In the case of Al_2O_3 substrate (TABLE 2), the single bump resistance extraction is about 0.9 m Ω . There is no observable variation on daisy-chain resistance with thermal cycling up to 300 cycles (for the results available at this date). The single bump resistance slightly increases with the cycles (about 3%).

Table 2 : EVOLUTION OF BUMP CONTACTS ON Al_2O_3 WITH TEMP. CYCLING

Cycles	Init.	100 c.	200 c.	300 c.
Daisy-Chain	1.56 Ω	1.56 Ω	1.56 Ω	1.56 Ω
std dev.	0.08 Ω	0.08 Ω	0.08 Ω	0.08 Ω
Failure	0/108	0/108	0/108	0/108
Single bump	0.88 m Ω	0.89 m Ω	0.91 m Ω	0.92 m Ω
std dev.	0.24 m Ω	0.24 m Ω	0.24 m Ω	0.24 m Ω

In the case of AIN substrate without underfill, a small variation is observed on the daisy-chain resistance but the single bump resistance is increased by a factor of 4 to 5.

That bonding degradation is clearly due to the higher mismatch between the coefficient of thermal expansion of GaAs and AIN than GaAs and Al_2O_3 substrates. The thermal cycles induce more stress on the GaAs chip and its bumps when bonded on AIN substrate than bonded on alumina.

At initial time, the single bump mean value is greater than with Al_2O_3 substrate, due to thermo-mechanical stress during cooling after bonding. 13 bumps are disconnected after 300 cycles, all located on the corner of the dices.

Table 3 : EVOLUTION OF BUMP CONTACTS ON AIN WITHOUT UNDERFILL WITH TEMP. CYCLING

Cycles	Init.	100 c.	200 c.	300 c.
Daisy-Chain	1.66 Ω	1.71 Ω	1.71 Ω	1.77 Ω
std dev.	0.03 Ω	0.07 Ω	- Ω	- Ω
Failure	0/72	1/72	9/72	13/72
Single bump	1.13 m Ω	1.70 m Ω	3.17 m Ω	4.58 m Ω
std dev.	0.25 m Ω	0.55 m Ω	3.0 m Ω	4.1 m Ω

In the case of AIN substrate with underfill, there is no observable variation on the single bump and daisy-chain measurements. Like without underfill, the initial time single bump resistance mean value is greater than with Al_2O_3 substrate, due to thermo-mechanical stress during cooling after bonding but only a very slight increase is observed after the thermal cycling.

Table 4 : EVOLUTION OF BUMP CONTACTS ON AIN WITH UNDERFILL WITH TEMP. CYCLING

Cycles	Init.	100 c.	200 c.	300 c.
Daisy-Chain	1.68 Ω	1.68 Ω	1.68 Ω	1.68 Ω
std dev.	0.03 Ω	0.03 Ω	0.03 Ω	0.03 Ω
Failure	0/36	0/36	0/36	0/36
Single bump	1.05 m Ω	1.06 m Ω	1.06 m Ω	1.07 m Ω
std dev.	0.34 m Ω	0.35 m Ω	0.35 m Ω	0.36 m Ω

These DC measurements demonstrate the compatibility of our flip-chip bonding process for GaAs MMIC on alumina substrate. Underfill is needed for the use of aluminum nitride substrate with 5 mm x 5 mm GaAs MMICs.

The daisy-chain demonstrators will be aged up to 1000 temperature cycles.

IV. RF AMPLIFIERS

A. Test Vehicle design

The bonding height is imposed to avoid any propagation disturbance at MMIC level. Electromagnetic simulations using the finite element software HFSS show that a 35 μm +/- 5 μm height for coplanar design is sufficient. For microstrip MMICs, the simulations show that influence of the host substrate would be higher so several heights (30, 60 and 90 μm) have been tested on a Ku microstrip amplifier.

TABLE 5 shows the impedance and electrical length changes due to the proximity of the host substrate (the bump height). The first simulation deals with a 50 ohms coplanar line of $W= 30 \mu\text{m}$ and $G=15.5 \mu\text{m}$ (typical value for MMICs implementation). The second simulation is about a 50 ohms microstrip lines on $100 \mu\text{m}$ thinned GaAs with $W= 72 \mu\text{m}$.

Table 5 : IMPEDANCE AND ELECTRICAL LENGTH CHANGES WITH BUMP HEIGHT

Bump height	Coplanar		Microstrip	
	Imp.	el. length	Imp.	el. length
0	-34 %	+34%	-21%	+20 %
10	-4.2 %	+3.9 %	-11	+7.8 %
30	-0.6 %	+0.5 %	-4 %	+2.5 %
50	-0.4 %	+0.2 %	-2.8 %	+1.3 %
100	0 %	0 %	-0.6 %	+0.6 %
200	0 %	0 %	0 %	0 %

On the test vehicle, the nominal $35 \mu\text{m}$ height is performed with double stacked stud bumps and nominal $295^\circ\text{C} / 30 \text{ g.}$ per bumps thermocompression bonding profile. The height variation study with the Ku microstrip MMIC is performed with single, double and triple stacked stud bumps and variation of the bonding force.

The RF amplifier Test Vehicles are of 4 kinds : LLA (Low Level Amp.) Ku and LLA Ka in coplanar design and LLA Ku and LNA Ka in microstrip design. The MMICs are rounded by the two coplanar access lines and by the DC decoupling networks. The geometry of the access lines is $W=70 \mu\text{m}$, $G=40 \mu\text{m}$ with an overall length of 5 mm.

B. RF results

All RF demonstrators have been manufactured, tested and aged 200 cycles in temperature. The total number of demonstrators is 8 LLA Ku coplanar, 5 LLA Ka coplanar, 11 LLA Ku microstrip and 13 LLA Ka microstrip (Fig. 1, 3).

The measurements showed very small degradation induced by the flip-chip bonding even for the microstrip design (Fig. 2, 4). The gain discrepancies are typically less than 1 dB between the initial on-wafer measurement and the flip-chip losses-corrected demonstrator.

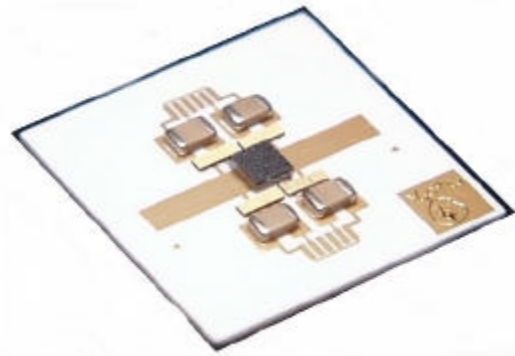


Figure 1 : Ku coplanar demonstrator view

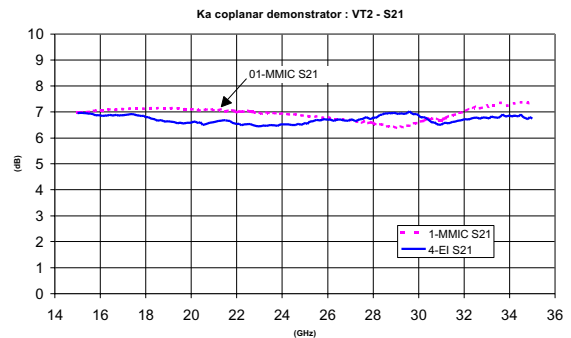


Figure 2 : Ka coplanar demonstrator results

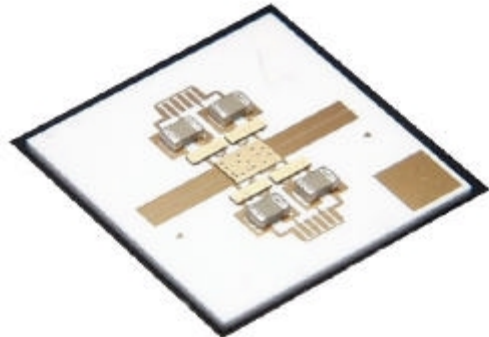


Figure 3 : Ku microstrip demonstrator view

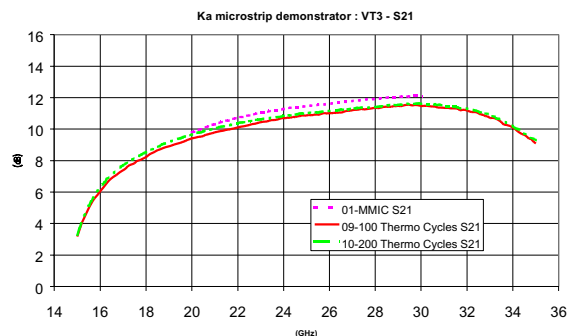


Figure 4 : Ka microstrip demonstrator results

Concerning reliability, the only 2 failures over 8 microstrip Ku demonstrators (one after fabrication and the other after 100 temp. cycles) have been identified. They can be attributed to a local pollution on a drain pad due to a careless handling. All others demonstrators have presented the same electrical response before, during and after aging.

The other very interesting result is that the microstrip Ku demonstrators bonded with 30 μm ; 60 μm and 90 μm bump height have presented the same electrical response. The slight observed differences are coming from dice to dice dispersion.

V. CONCLUSION

This study demonstrates the compatibility of on-the-shelves MMICs with flip-chip bonding, even with microstrip design and the reliability of gold-gold thermocompression bonding of GaAs MMICs with gold stud bumps on alumina without underfill. The effect of this mounting on the microwave response is only in the order of few tenth of dB losses, allowing the use of existing MMICs for both microstrip and coplanar designs.

Underfill is necessary for the use of aluminum nitride substrate for power applications. In that case, specific MMIC design or active-side specific treatment can not be avoided due to the too high value of the underfill dielectric constant.

VI. ACKNOWLEDGMENTS

A part of this work has been supported by the CNES (French Space Agency) and the DGA (French DoD).

The authors would like to thank M. Aufrere and J.L. Badoch for the DC and RF measurements.

VII. REFERENCES

- [1] M. Vrana, J. De Baets, A. Van Calster, B. Allaert "Flip chip Assembly for Chips with Gold stud Bumps on High Density Thick Film Substrates", in 11th European Microelectronics Conference, May 1997
- [2] C. Drevon, S. George, A Coello-Vera "Flip-chip with MMICs on the shelves", in Advanced Packaging Materials Symposium - Flip-chip Workshop, March 1999
- [3] D. Roques, S. George, J-F. Villemazet, B. Cogo, C. Drevon "Impact du montage flip-chip sur les MMICs", in 3^{ème} Journée d'Electromagnétisme et Microondes de Toulouse, Jan. 2000