Finite Ground Coplanar Waveguide Shunt MEMS Switches for Switched Line Phase Shifters

George E. Ponchak, Rainee N. Simons, Maximilian C. Scardelletti, and Nicholas C. Varaljay

NASA Glenn Research Center
21000 Brookpark Rd., MS 54/5
Cleveland, OH 44135
TEL: 216-433-3504, FAX: 216-433-8705
George.Ponchak@grc.nasa.gov

Abstract **-** Switches with low insertion loss and high isolation are required for switched line phase shifters and for transmit/receive switches at the front end of communication systems. The design, fabrication, and characteristics of a Finite Ground Coplanar (FGC) waveguide capacitive shunt MEMS switch implemented on high resistivity Silicon is presented. The switch has a measured insertion loss and return loss of less than 0.35 dB and greater than 11 dB respectively, over the frequency range of 3 to 50 GHz. The measured isolation is greater than 18 dB at 50 GHz.

I. INTRODUCTION

NASA, military, and commercial satellites use phased array antennas to optimize satellite performance by steering and shaping the radiation pattern. Phased array antennas are also used for scanning radar systems in terrestrial systems. The enabling component in phased array antennas is the phase shifter. However, the insertion loss of GaAs MESFET, switched line phase shifters is too high for many applications and forces system designers to use more amplifiers which greatly complicates thermal management.

To solve these problems, RF MEMS switches have recently been developed. These include rotary MEMS switches [1], single supported cantilever MEMS switches [2], and capacitive membrane MEMS switches [3,4]. Capacitive membrane MEMS switches rely on electrostatic force to pull a double supported cantilever beam down and provide an RF short between the signal line and the ground plane.

In this paper, we present the design, fabrication, and characterization of a Finite Ground Coplanar (FGC) waveguide capacitive shunt MEMS switches. The switch fabrication relies on standard air bridge processing and is thus fully compatible with SiGe/Si monolithic integrated circuit processing. Moreover, because the processing is not dependent on the substrate, the switches may also be fabricated on GaAs, glass, or other microwave substrates.

II. SWITCH DESIGN

Figure 1 shows a schematic of the Type I, FGC waveguide capacitive shunt MEMS switch. The switch is implemented in FGC waveguide with center strip conductor width (S), slot width (W), and ground plane width (G) of 50, 35, and 150 μm respectively, which yields a characteristic impedance of 50 Ω. A dielectric (Si_3N_4) covers the center strip conductor and ground planes of the FGC waveguide. The dielectric prevents stiction between the bottom electrodes and the cantilever when they come into contact. Because the FGC waveguide is electrically and physically narrow, the doubly supported cantilever spans the entire width of the transmission line. In addition, the two supporting pads are separated from the transmission line by a 10 μm gap. Thus, the bias voltage applied to the cantilever is isolated from the transmission line.

When the cantilever is in the UP position, the parallel plate capacitance between the metal membrane and the bottom electrode, C_{OFF}, is small and the switch behaves as an open circuit. Hence, the signal transmission through the switch takes place with low insertion loss. In this state, the switch is said to be OFF. Conversely, when the cantilever is in the DOWN position, the parallel plate capacitance between the metal membrane and the bottom electrode, C_{ON}, is large and the switch behaves as a short circuit. Hence, the signal is reflected back and the insertion loss is very high. In this state, the switch is said to be ON.

Cantilevers are built with and without 10 μm square holes. The holes help in the removal of the sacrificial layer under the cantilever if a plasma dry release process is used. The hole dimensions were arbitrarily chosen as 10 μm. For a given FCG waveguide dimensions, the length L_m is fixed. Hence, to investigate the effect of switch geometry on C_{ON} and C_{OFF}, several switches with width W_m in the range of 90

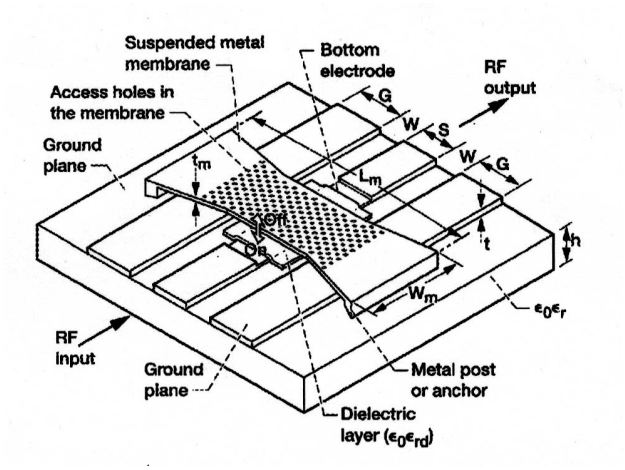

Figure 1: Schematic of the Finite Ground Coplanar Waveguide capacitive shunt MEMS switch.

to 250 μm are fabricated. A SEM picture of a typical MEMS switch investigated is shown in Figure 2.

Figure 3 shows an SEM of the Type II, FGC waveguide capacitive shunt MEMS switch configuration. In this configuration, the cantilever is formed by elevating the FGC waveguide center strip conductor above the substrate. An under-pass ties the ground planes together. When compared to the Type I switch, the cantilever in this design is much smaller and hence the switch is very compact. However, the disadvantage is that the bias voltage has to be applied between the center strip conductor and the ground planes and hence might interfere with other semiconductor devices in a practical circuit.

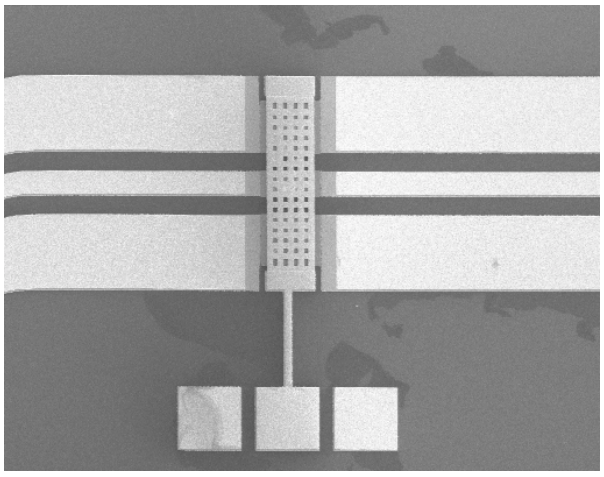

Figure 2: SEM image of Type I, FGC waveguide capacitive shunt MEMS switch.

III. SWITCH FABRICATION

The fabrication process, which is common to both Type I and II switches, is schematically illustrated in Figure 4. The RF switches are fabricated on a high resistivity Silicon wafer, (ρ>2500 Ω-cm and h ≈ 400μm) with 450 nm of thermally grown SiO_2, which electrically isolates the bias lines from the FGC waveguide. First, the underlay metal comprised of 20 nm of Cr and 1000 nm of Au is defined through standard lift-off processing. Second, 200 nm of PECVD Si_3N_4 is grown on the wafer and patterned by Reactive Ion Etch (RIE) to isolate the cantilever from the FGC waveguide when the switch is in the down state. Third stage lithography is then used to define the sacrificial photo resist layer under the cantilevers. Following this 250 nm of Au is RF sputtered onto the wafer. This forms the seed layer for the Au electroplating. Fourth stage lithography is performed to define transmission lines and cantilevers, which are electroplated to a final thickness of 1.5 um. Fifth, the photoresist and seed layers are removed. Finally, the sacrificial layer is removed by super critical dry release method leaving behind a metal membrane, which is approximately 1μm thick.

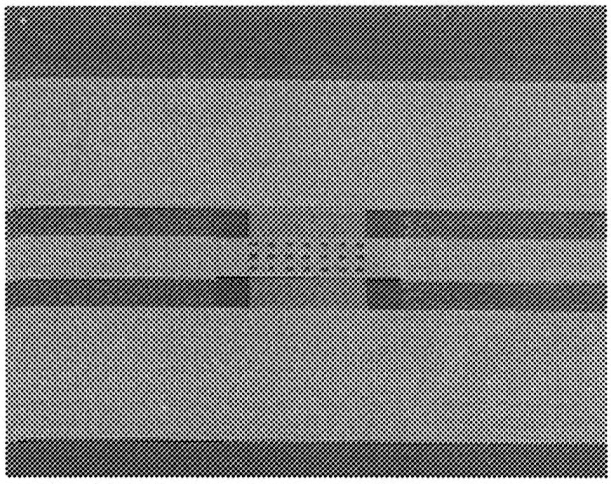

Figure 3: SEM image of Type II FGC waveguide capacitive shunt MEMS switch.

IV. MEASUREMENTS

The switches are characterized on an HP8510 vector network analyzer using GGB Industries RF G-S-G probes. Between the Silicon wafer and the probe station wafer chuck, a quartz plate is used to isolate the circuits and prevent parasitic modes. In this paper, the measurements carried out on Type II switches are only reported. The bias is applied between the center strip conductor and the ground planes of the FGC waveguide through a coaxial bias tee. A Thru-Reflect-Line (TRL) calibration is implemented through the NIST MULTICAL software routine [5], with the calibration standards fabricated on the same wafer as the switches. Thus, the reference plane is at the edges of the switches.

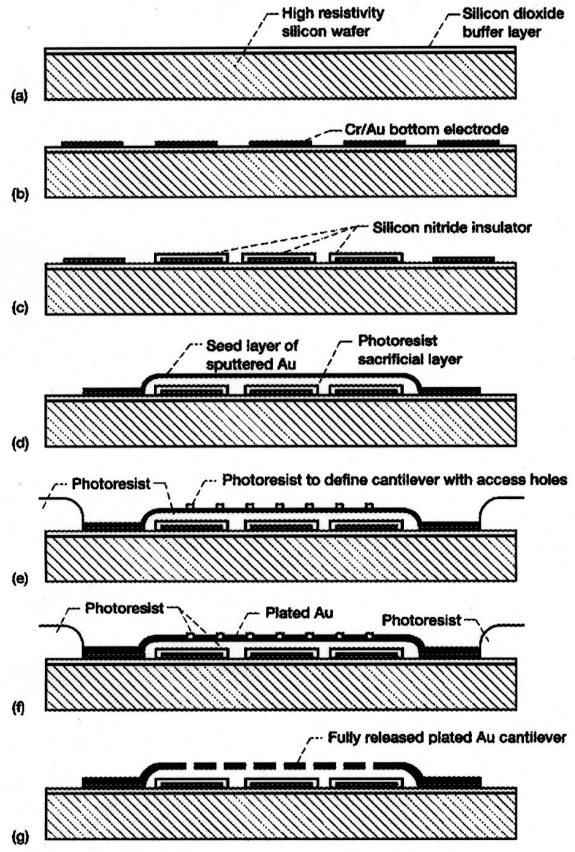

Figure 4: Fabrication process for Type I and II FGC waveguide capacitive shunt MEMS switch.

Probe placement repeatability limits insertion loss measurement accuracy to 0.1 dB.

V. EXPERIMENTAL RESULTS AND DISCUSSIONS

Visual inspection reveals that, the switches exhibit signs of excessive stress as evidenced by a slight bowing of the cantilever. This stress also resulted in a higher pull down voltage than what was predicted; the pull down voltage is 35 V for Type II switch. In our initial experiments, the bias consisted of a DC voltage source. However, with this type of source, we were not able to control the switch activation. When the DC voltage source was replaced by a 60 Hz half-wave rectified supply, a controllable switch activation was achieved. We believe the charging of the dielectric layer causes this phenomenon and is under further investigation.

The RF characteristics of the Type II switch in the UP or OFF state are shown in Figure 5. The switch has an insertion loss of less than 0.35 dB and a return loss greater than 11 dB over the frequency range of 3 to

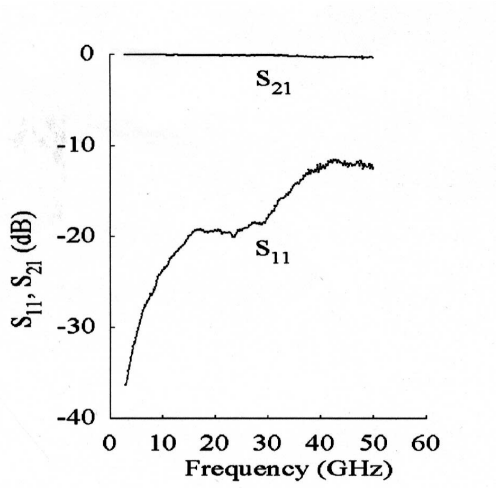

Figure 5: RF characteristics of the Type II, FGC waveguide capacitive shunt MEMS switch in the UP or OFF state, membrane length is 90 μm.

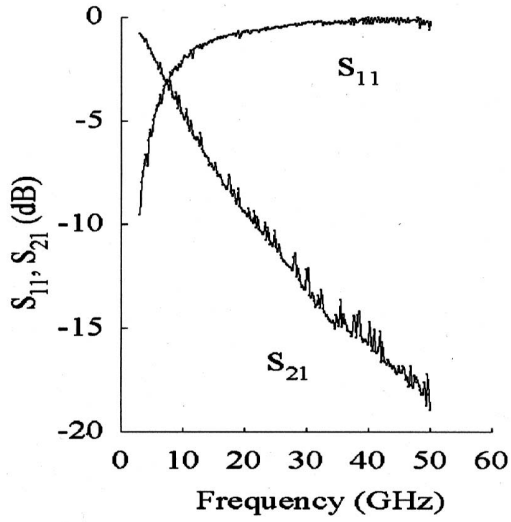

Figure 6: RF characteristics of the Type II, FGC waveguide capacitive shunt MEMS switch in the DOWN or ON state, membrane length is 90 μm.

50 GHz. The RF characteristics of the Type II switch in the DOWN or ON state are shown in Figure 6. The switch has an isolation greater than 18 dB at 50 GHz.

VI. CONCLUSIONS

FGC waveguide capacitive shunt MEMS switches have been fabricated on high resistivity Silicon using standard air bridge processing. The switch has an insertion loss and return loss of less than 0.35 dB and greater than 11 dB respectively, across the frequency range of 3 to 50 GHz. The isolation is greater than 18

dB at 50 GHz. These switches offer the potential to dramatically improve phase shifter performance, which will enable lower cost, simpler phased array antennas.

Acknowledgement

The authors are grateful to Gary Lesney for the design and fabrication of the DC power supply for activating the MEMS switches.

REFERENCES

1. L. E. Larson, R. H. Hackett, M. A. Melendes, R. F. Lohr, "Micromachined microwave actuator (MIMAC) technology-a new tuning approach for microwave integrated circuits," *IEEE 1991 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest*, pp. 27-30.
2. D. Hyman, A. Schmitz, B. Warneke, T. Y. Hsu, J. Lam, J. Brown, J. Schaffner, A. Walston, R. Y. Loo, G. L. Tangonan, M. Mehregany, and J. Lee, "GaAs-compatible surface-micromachined RF MEMS switches," *Electronics Letters*, Vol. 35, No. 3, pp. 224-225, Feb. 4, 1999.
3. S. P. Pacheco and L. P. B. Katehi, "Microelectromechanical K-band switching circuits," *29th European Microwave Conference Digest*, 1999, pp. 45-48.
4. Z. J. Yao, S. Chen, S. Eshelman, D. Denniston, and C. Goldsmith, "Micromachined low-loss microwave switches," *IEEE Journal Microelectromechanical Systems*, Vol. 8, No. 2, pp. 129-134, June 1999.
5. D. F. Williams, R. B. Marks, and A. Davidson, "Comparison of on-wafer calibrations," *38th ARFTG Conf. Dig.*, San Diego, CA, Dec. 5-6, 1991.