# SELF CONSISTENT MODELLING OF PHEMT DEVICES FOR MILLIMETER WAVE SMALL SIGNAL, NOISE AND POWER APPLICATIONS.

D M Brookbanks

Marconi Caswell Ltd, Caswell, Towcester, Northants, NN12 8EQ, UK
*e-mail: mike.brookbanks@gecm.com*

## ABSTRACT

Accurate simulation of PHEMT based GaAs MMIC's requires a bias dependent model that can be used in both small signal and large signal analysis and is accurate over a wide range of applied bias. The majority of models that are supplied with the commercial high frequency simulators have limitations that prevent this goal being achieved. The model areas that require attention are the symmetry of the model at drain-source voltages close to zero, use of the correct time delays within the device and a more precise inclusion of the bias dependent intrinsic noise processes. In this paper an approach to the generation of a large signal model is described that attempts to reconcile these requirements.

## INTRODUCTION

Many MMIC circuits use active component topologies where the bias voltages on the devices can not be determined a-priori and a DC analysis is required to evaluate the voltages that are applied to the active device terminals. Typical examples are self-biassed low noise amplifiers and cascode stages. A DC analysis of the circuit can then be carried out to determine the operational bias points of each device. Once these device voltages have been determined small signal S-parameter and noise figure analysis can be undertaken if the suitable S-parameter files or models are available at the bias points. This method is inefficient as the DC and AC analyses are decoupled and it may require access to a large number of measured S-parameter sets if scaleable device models are not available. What is required is a non-linear model that can provide a suitably accurate description of the device as a function of both frequency and the terminal voltages allowing a single analysis to determine the performance of the circuit.

The starting point for this modelling is to generate a non-linear model that has the same topology as the small signal linear model that is used to describe the individual device so that in the small signal limit the correct S-parameters will be generated. This will lead to a solution of the problems identified above and also create a model that is capable of providing more accurate large signal analyses. Many of the models that are available in the commercial simulators, (for example the EEFET3/EEHEMT1 [1] models in Libra® from Agilent Technologies) reduce to the commonly used small signal equivalent circuit model. In many cases this topology is unable to provide an adequate description of the device at high frequencies. In addition these simulator models may not have the correct symmetry at Vds=0 for switch applications and have a restricted built in noise model.

## SMALL SIGNAL MODELS

It has been found that the standard small signal equivalent circuit model that has been used for many years is not capable of providing a sufficiently accurate description of the MCL PHEMT at high drain bias and high frequencies. This is illustrated in Figure 1 where there is a divergence in the fit to S22 and a difference in the reverse feedback S12. This data is for an 8*60µm device biassed at Vds=8.0V and Vgs=-0.4V. Some of this difference can be overcome by allowing the source and drain resistances $R_s$ and $R_d$ to become negative. This is of course non-physical but it is a result of the limitations of the standard equivalent circuit model. Whilst this approach can be used for small signal analysis, where the only requirement is to replicate the S-parameters, the method can not be used for large signal or noise analysis where the parasitic resistances *must* be positive. Even for small signal S-parameters this solution can only be used over a limited frequency range as the negative resistances can lead to an extrapolated S22 that is greater than unity. A considerable improvement can be achieved by the inclusion of two additional elements to the equivalent circuit model. The first of these is the inclusion of the capacitance Cdc, which is commonly referred to as the dipole domain capacitance, and the second is to introduce a time delay to the output conductance Gds. The capacitance Cdc used to be a feature of MESFET models but is not commonly used in current models. It can

be shown that the inclusion of Cdc, in conjunction with the gate charging resistance $R_i$ and the transconductance delay $\tau$, leads to a negative resistive contribution to S22 as required by some of the FET model fitters. If the contribution from $R_i$ is ignored then Cdc will appear as a capacitor in parallel with Cds and it is not required in the equivalent circuit. When Cdc is included in the equivalent circuit the value of Cds is reduced and corresponds to the geometric capacitance associated with the drain-source metallisation. The inclusion of these two additional elements enables a good model fit to be obtained whilst maintaining the parasitic source and drain resistances at physically realistic values. The addition of a time delay to the output conductance was introduced on the basis of symmetry with the transconductance; this component is also a feature of the MESFET equivalent circuit in the Harmonica® simulator from Ansoft [2]. The use of an output conductance delay to improve the compatibility between small and large signal modelling has also been presented by Strubble et al [3]. Both the drain (output conductance) and gate (transconductance) delays increase significantly at high drain bias and have to be taken into account if accurate modelling is to be achieved. In the saturated region the drain delay exceeds the gate delay. For the PHEMT considered above both delays are approximately linearly dependent on the drain-source voltage and only slightly dependent on the gate-source voltage. At a drain-source voltage of 5V typical values are $\tau_{gm}$=2.5ps and $\tau_{ds}$=3.5ps. Figure 2 compares the results of this extended model with the original data showing a considerably better fit to the data. In contrast to the original model this model will extrapolate to higher frequencies. The improvement in the fit to S22 can be clearly seen. This arises from the fact that the delays that are associated with the drain current are becoming a significant fraction of the RF period at the highest frequency. For power devices that may operate at drain voltages in excess of 7 volts these delays must be taken into account if accurate simulations are to be made, as there may be significant phase delays at the harmonic frequencies when designing millimeter wave amplifiers.

## NON-LINEAR MODELS

By using the user defined model capability in Libra® the topology of the non-linear model can be changed to include these two additional components and provide consistency between the large-signal and small-signal simulations. The basic model used was based upon the Libra EEHEMT1 non-linear model with the addition of a fixed capacitor Cdc and the introduction of two bias dependent time delays. $Vgs'=Vgs(t-\tau_{gm})$ and $Vds'=Vds(t-\tau_{ds})$. This implementation of the model was stable and allowed simulations even when the device was well into compression. In the small signal limit the predicted S-parameters agreed well with those of the extended equivalent circuit model shown in Figure 2.

The EEFET3/EEHEMT1 models provide analysis for Vds<0 by using the same model equations for Vds>0 but with Vds replaced with -Vds and Vgs replaced with Vgd. These substitutions lead to a lack of symmetry in the characteristics close to Vds=0 which can be a problem if devices such as switches are required. This can be overcome by reformulating the equations in terms of the voltages Vgs and Vgd so preserving the physical symmetry of the device in the mathematical model. As an adjunct to this the use of two time delayed control voltages Vgs' and Vgd' provide the self consistency required with the small signal model. These modifications have also been compiled into the user-defined non-linear model in Libra®. Figure 3 shows a comparison between the output conductance that is predicted by the EEHEMT1 model and the new MCL user defined model as the drain-source voltage is swept from –1.0V to 1.0V. The lack of symmetry in the EEHEMT1 model can be clearly seen. The slight lack of symmetry in the MCL model arises from the fact that the physical construction of the device has the gate closer to the source than the drain leading to an increase in the drain parasitic resistance. When the effective source and drain terminals are swapped, by reversing the drain-source potentials, this leads to an asymmetry in the internal bias applied to the device.

The MCL model also contains the parasitic resistances and inductances that are an integral part of the device allowing the device model to be used in a scaleable mode.

## NOISE MODELS

When used in MMIC LNA circuits the non-linear model must be capable of describing the noise performance of the PHEMT at the DC bias conditions that the device sees at that point in the circuit. For example in feedback circuits the actual DC operating point may depend on the resistive elements that form part of the feedback network. The EEFET3/EEHEMT1, and many other, non-linear models use a fairly

simple noise model that is common in SPICE simulators where the intrinsic noise in the device is modelled as a drain noise current source with the following spectral density:

$$\frac{< i_{ds}^2 >}{\Delta f} = \frac{8kTg_m}{3}$$

This does not adequately represent the noise in the real PHEMT for a number of reasons. Firstly the correlation's that exist between the gate and drain noise sources are not included and, secondly the drain noise is assumed to be thermal in origin, whereas the actual drain noise is fairly insensitive to the ambient temperature as the mechanism is not thermal in origin. Finally the transconductance is not the ideal parameter with which to characterise the noise as this reduces to zero at Vds=0 when the channel in fact becomes a resistor, which definitely generates ambient temperature noise. This final point is important, as this can be a significant source of noise in a network that uses PHEMT based switches such as the diversity switch at the input of a transceiver.

Figure 4 shows the effective temperature (the noise output conductance * Rds) of the drain noise for an MCL PHEMT. The effective temperature is reasonably independent of drain bias once this exceeds the saturation knee and reaches its minimum value when the drain current is ~30% of Idss. Below the saturation knee the effective temperature is tending to unity as would be expected.

These features have been included in the MCL compiled non-linear model in Libra® in order to create an improved bias dependent noise model for circuit simulation. Figures 5 and 6 compare the measured and modelled minimum noise figures for a 4*40μm PHEMT. Given that the drain noise temperature can be assumed to be independent of the drain bias, the drain noise model depends only upon the drain current (or Vgs). The gate noise voltage was found to be independent of the drain voltage and is also modelled as a function of the Vgs only. The correlation between the gate and drain noise currents can be taken to be purely imaginary. At Idss the correlation coefficient was ~j0.61 and the correlation coefficient increased until the noise sources were almost totally correlated as pinch off was approached. A smoothing function based on the linear to saturation regions of the I/V characteristics was applied to the drain noise to move from a high temperature independent noise temperature in the saturation region to an ambient temperature resistive noise source at Vds=0. Once these noise currents have been determined the simulators internal function calls can be used to add the noise currents to the noise correlation matrix in order to determine the overall noise performance of the circuit.

## CONCLUSIONS

In this paper the changes that are required to both small signal and large signal models of a MESFET/PHEMT that are necessary to provide accurate millimeter wave simulation have been discussed. The proposed model changes provide a self-consistency between the linear and non-linear models and enable accurate noise figure simulations to be carried out. By ensuring that the inherent physical symmetry of the device is taken into account in the mathematical model some of the problems that have been experienced in the low voltage region have also been overcome.

## ACKNOWLEDGMENTS

The work presented has primarily been funded by Marconi plc with additional support from DERA and BAE SYSTEMS

## REFERENCES

[1] Series IV/PC, Release 6.5, Circuit Network Items Manual, Ch 10 pp61-110
[2] Microwave Harmonica, Version 7.x P.C., Elements Library,Ch 2 pp72-76
[3] W. Strubble, A. Platzker, S. Nash and J. Pla, "A New Small Signal MESFET and HEMT Model Compatible With Large Signal Modelling", *IEEE MTT-S Digest*, pp1567-1570, 1994

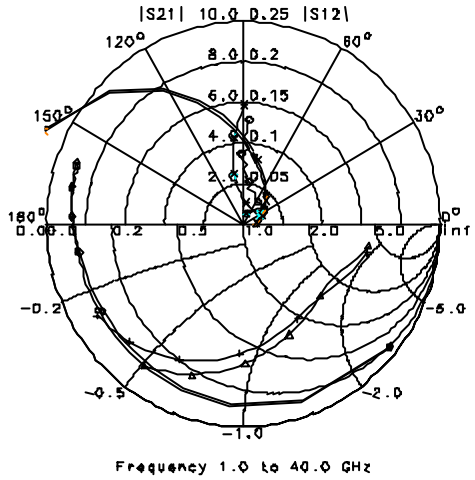


Figure 1 PHEMT S-parameters fitted using the 'standard' equivalent circuit.

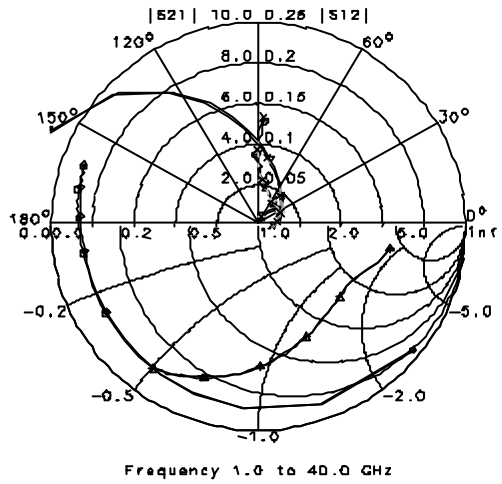


Figure 2 PHEMT S-parameters fitted using the 'improved' equivalent circuit.

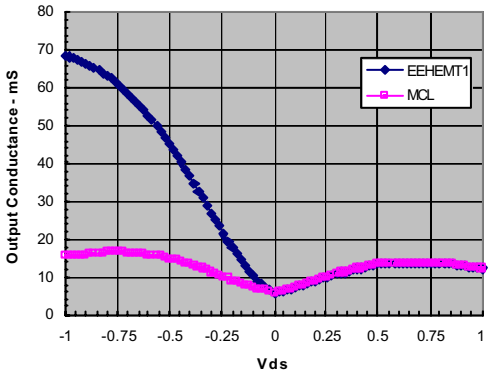


Figure 3 PHEMT Output Conductance (Gds) for two large signal models.

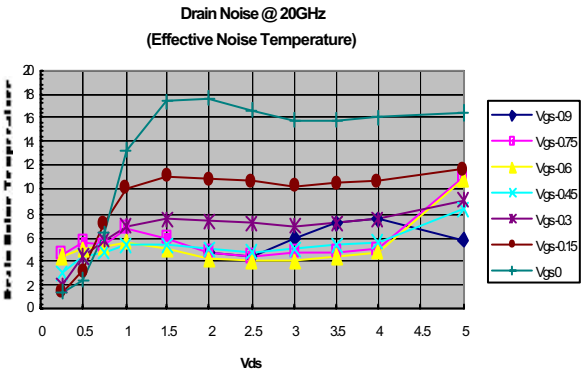


Figure 4 Drain Noise Temperature (Td/290) for an MCL 4*40µm PHEMT

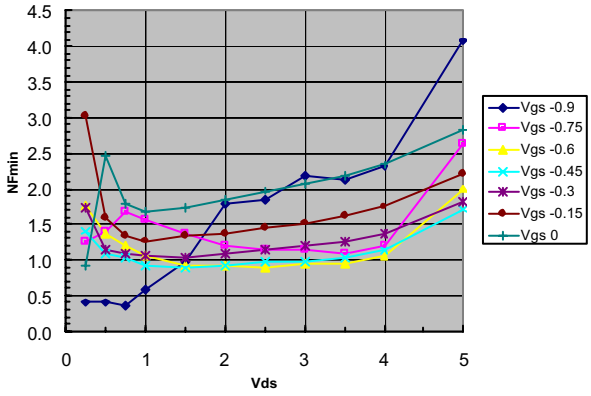


Figure 5 Measured Minimum Noise Figure for an MCL 4*40µm PHEMT as a function of gate and drain bias.

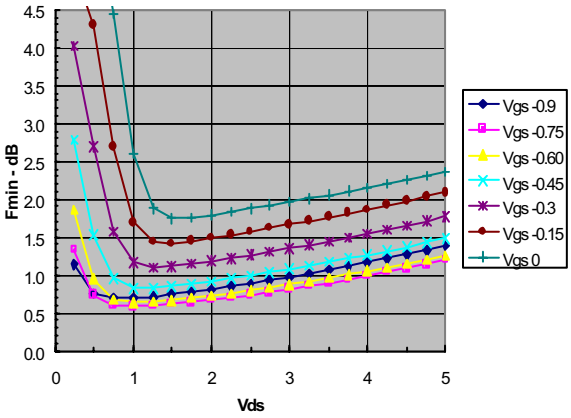


Figure 6 Predicted Minimum Noise Figure for a 4*40µm PHEMT using the MCL large signal model