Gate ionization current of an Enhancement-Mode metamorphic $Al_{0.67}In_{0.33}As/Ga_{0.66}In_{0.34}As$ HEMT on GaAs substrate

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Abstract

This paper presents original results provided by combination of Enhancement-Mode (E-mode) with metamorphic growth of $Al_{0.67}In_{0.33}As/Ga_{0.66}In_{0.34}As$ HEMT structure on a GaAs substrate. The devices, which are the first reported for Enhancement-Mode $Al_{0.67}In_{0.33}As/Ga_{0.66}In_{0.34}As$ MM-HEMT's, exhibits good dc and rf performance. Good Schottky characteristics have been obtained (a forward turn-on voltage of 0.9V and a typical reverse gate to drain breakdown voltage of 16 V). The 0.4µm gate length devices have a saturation current of 455 mA/mm at +0.8V gate voltage. Gate current studies, versus gate-to-drain extension have been observed, in the first time, in such as devices, showing gate current issued from impact ionization.

1-Introduction

The Enhancement mode device is interesting since it eliminates the need for a negative voltage supply on a chip. Recent works on E-mode AlInAs/GaInAs HEMT's on InP substrates have demonstrated superior microwave and low noise performance over Pseudomorphic HEMT's on GaAs substrates [1,2]. GaAs substrates are more suitable for large scale MMIC production contrarily to InP substrates which are fragile, difficult to etch, not available in large scale and more expensive. A way to avoid InP substrate is to use metamorphic (MM) buffers to accommodate the lattice mismatch between the active layer and the GaAs substrate. We have used an inverse step-graded buffer of AlInAs [3,4,5] and we benefit of the indium composition close to 30% for power application. The high ΔE_c of 0.7 eV leads to high sheet carrier density and good confinement [5]. The high bandgap of InAlAs and InGaAs as compared to higher indium content allows respectively a good Schottky barrier height that improves breakdown voltage and reduces the impact ionization.

2-Device processing

The layers were grown on (100)-oriented GaAs substrate using a Riber 32P Molecular Beam Epitaxy machine. *Figure 1* show the simple heterostructure. The fabrication started with the realization of source and drain ohmic contacts. For the ohmic contact formation, using Ge/Au/Ni/Au metalisation and rapid thermal annealing at 340°C during 60s under N_2/H_2. TLM (Transmission Line Model) measurements show a typical ohmic contact resistance R_c of 0.20 Ω. Device isolation was performed by non selective chemical mesa etching down to the AlInAs buffer layer with $H_3PO_4/H_2O_2/H_2O$ (5:1:40) etchant. The T-gate was defined using a bilayer resist (PMMA / P(MAA-MAA)) to improve lift-off. After the chemical recess using a selective etchant (succinic acid / H_2O_2) [6], the gate metallisation is e-beam evaporated and consists of Ti/Pt/Au sequence. The etching selectivity ratio of InGaAs over AlInAs was greater than 500. Typical Schottky characterization gives an ideality factor η of 1.7 and a Schottky barrier height Φ_b of 1.275 eV. As the final step, thick Ti/Au contacts were deposited for microwave probing pads.

3-Experimental results

DC and microwave characteristics of 100µm wide MM-HEMT's were measured on wafer. The *I-V* characteristics are given in *figure 2* and *figure 3*. The devices exhibit a drain-to-source current I_{DS}= 455 mA/mm at a gate-to-source voltage V_{GS} = +0.8 V. The pinch-off voltage V_P is -0.45V. Typical extrinsic transconductance and output conductance are 496 mS/mm and 13.5 mS/mm which gives an extrinsic gain voltage gm/gd of 38. Hall effect measurements are used to determine the sheet carrier density n_H and the electron mobility μ_H. They are, respectively, $3.9x10^{12}cm^{-2}$ and 7000 $cm^2/V.s$ at room temperature (300K).

S-parameter measurements were carried out and current gain cut-off frequency f_T were estimated. An extrinsic current cut-off frequency f_T of 62GHz and cut-off frequency f_{MAG} of 210GHz are achieved with the 0.4µm gate length device. They have been obtained at maximum transconductance bias condition (V_{DS} = 2 V and V_{GS} = 0 V). The Schottky characteristic curve for device with L_g = 0.4 µm is shown at *figure 4a*. A forward turn-on voltage of 0.9 V and a typical gate–to-drain voltage of –16 V at the gate current of 500 µA/mm were obtained. The good results in the Schottky diode are in a large part attributed to well controlled recess process. We processed devices with three source-to-drain extensions (L_{SD} =1 .3µm, 1.8µm and 3µm). We fixed the gate at 0.5µm from the source pad. We obtain a constant source resistance of 4.1Ω. Small signal equivalent schema extracted from measures show a C_{GS} of 328fF as expected and a decrease of C_{GD} versus L_{SD} (from 124 to 9,2 fF). The *figure 4b* shows the gate current characteristic for a source to drain extension of 3µm. At pinch-off channel ($V_{GS}<V_P$), we show the current issued of tunneling effects. It is very small because we have a large diode breakdown voltage whereas at open channel, we see ionization impact current. At V_{DS} = 4.5V, it reached 5µA/mm. So, it is the first time that we obtain such as figure in these devices. Also, the devices can not be biased at V_{DS} = 4.5V without main risk of irreversible damage. Therefore, devices present small ionization impact current before degradation which is attributed to a large ΔE_V of structure which prevents holes generated from ionization impact flowing thought the gate. This implies that these currents can hardly be observed when the Schottky diode is leaky. This explains that no similar experimental results has ever been published. *Figure 5* show the gate current characteristic at V_{DS}=3.5V. The lower ionization impact current for large L_{SD} implies that we have a decrease of electric fields peaks which spread into the structure.

Measurements at X-band on a load-pull power set-up were performed. Output power increase with extension. We have at 3dB gain compression a variation from 6.9dBm(30mW/mm) to 9.4dBm (75 mW/mm). Concerning power saturation, we remarks that the large is the extension, the higher is the saturation power (40mW/mm for a narrow extension and 110mW/mm for a large extension).

A simple explication can be done by the fact that the far is the drain pad, the higher is the drain resistance value. So, for a same drain current, we have a stronger fall-off of potential at the edge of the recess area beside drain corresponding to a electric fields peaks drop. So, it implies lower gate current. Also, great power value of large extension can be attributed to a better excursion of the signal compared to a narrow extension which have a precoce ionization voltage whereas for large extension, we have a better breakdown voltage (V_{DS}=4.5V).

4-Conclusion

Metamorphic devices exhibit good Schottky diode breakdown voltage. Our result strongly suggests that the optimization of the gate to drain extension will improve output power. These results are the first reported combining the E-mode and the metamorphic growth with this indium composition, present better results as compared to those with an indium composition of 50% [7] in term of breakdown in transistor operating and output power in X-band. It is clearly shown that the larger is the gate to drain extension, the higher is the output power because the signal benefit of

better drain-to-source voltage excursion with lower gate current which is responsible of degradation of devices. Also, the great interest of MM-HEMT over PM-HEMT by the superiority of the electron transport properties due to the high relaxation rate and the good filtering of dislocations is confirmed

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Figure captions

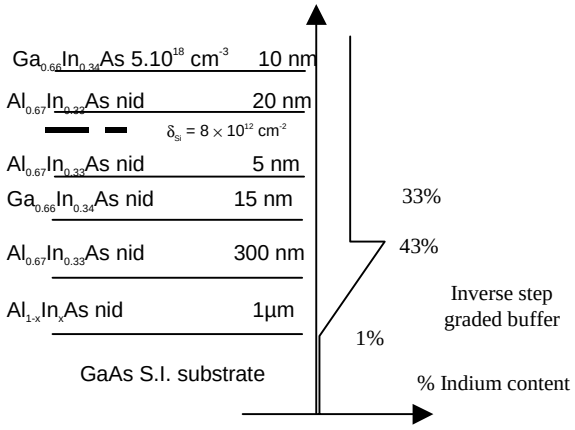

Figure 1 : Schematic of Simple Heterostructure-HEMT on GaAs substrate with the indium composition profile

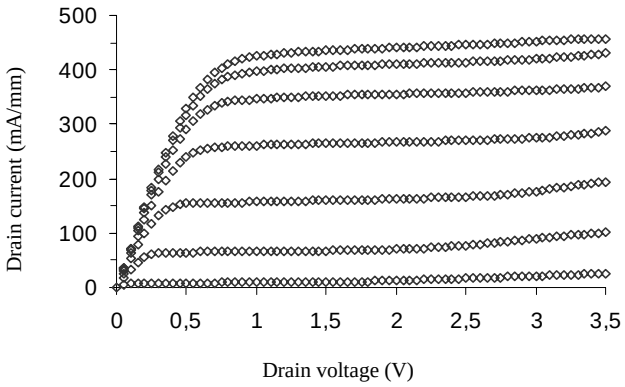

Figure 2 : DC characteristic of a E-Mode MM-HEMT. The gate voltage maximal is +0.8V, the step is .0.2V

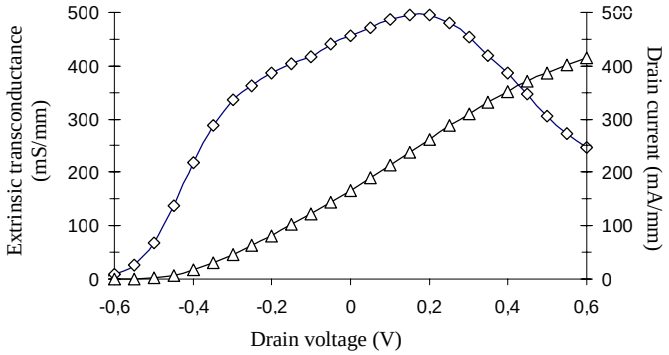

Figure 3 : Extrinsic transconductance and drain current versus gate voltage.

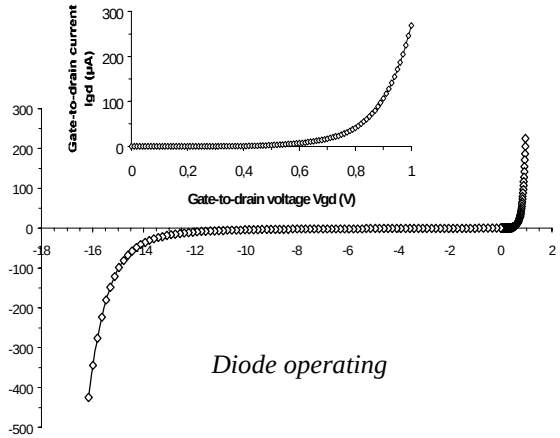

Figure 4a: The upper inset represents the forward Schottky characteristic and the central figure represents the complete characteristic

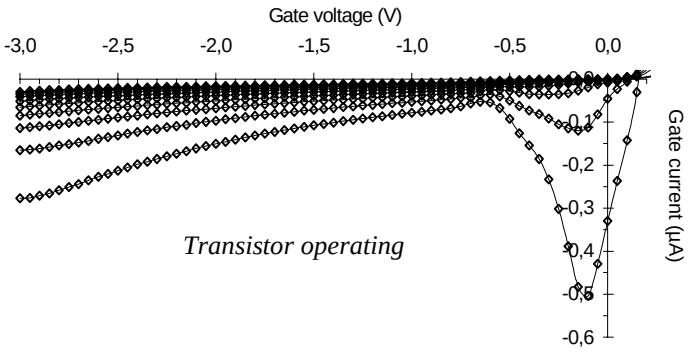

Figure 4b: Gate current characteristic for a large extension (V_{DS} varying from 1.5V to 4.5V with a step of 0.5V).

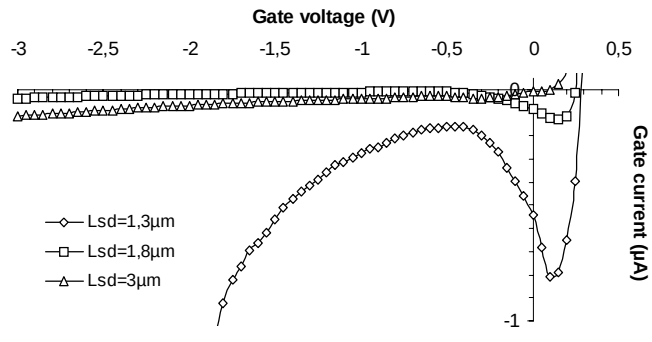

Figure 5 : Gate current versus gate voltage for different source to drain extensions.