SELF-ALIGNED GATE TECHNOLOGY FOR ANALOGUE AND DIGITAL GaAs INTEGRATED CIRCUITS

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PURPOSE OF THE WORK

Self-aligned gate technology for the fabrication of analogue and digital integrated circuits on GaAs has received much interest in recent years because of its potential for enabling high performance mono and multi-functional components with high yield /throughput capability. This technology is already being used in many foundries world-wide and is foreseen as the basis for next generation electronic sub-systems on GaAs.
The overall objective of this research is to develop an advanced technology for the fabrication of GaAs monolithic integrated circuits based on "self-aligned" transistors SAGFET's and/or SAGHEMT and utilise said technology for the fabrication of high performance, low cost mono and multi-functional analog/digital integrated circuits.

OUTLINE OF THE WORK

To achieve the above objective the research programme foresees the development of these synergic activities:

- development of a planar technology to fabricate SAGHEMT's device
- development of reliable electrical models of the devices by means of appropriate r.f. characterisation and subsequent design of mono and multi-function integrated circuits
- fabrication of mono and multi function integrated circuits to be fabricated as demonstrators the overall research activity.

Technology for the fabrication of high performance multi-function integrated circuits, is based on heterostructure active layer. Amplifiers, phase-shifters, digital circuits and TTL controlled Phase-shifter will be fabricated with the developed SAGHEMT's technology.

MAIN TECHNOLOGICAL RESULTS

We have developed a planar SAGHEMT's technology as described in figure 1. The main step of our process, are:

1. Optimisation of a metallic layer for Schottky contact, able to sustain high temperature as 600°C
2. Optimisation of a metallic layer for Ohmic contact able to penetrate epitaxial layer (GaAs/AlGaAs)

This new technology will ensure:
1.Active channel fabricated on epitaxial substrates with very high mobility (2 DEG channel)
2.Very low resistivity ohmic contact
3.Reduce channel length
4.Reduce access resistance

Therefore we will develop new devices, with very high performance yield and reproducibility, qualified for multifunction MMICs production

In figure 2 we have shown the employed gate structure, which is able to sustain self align ohmic contact process. It is possible to recognise a thick plated gold layer over a thin WN layer (b) and reduced channel length (a). In figure 3 we present some preliminary result obtained for epitaxial SAGFET as compared with convectional MESFET.

DEVICE MODELLING

Linear and non-linear models of the low-level and power SAGFET devices have been developed for inclusion in CAD simulation tools. The equivalent circuits have been extracted from multi-bias S-parameters and I/V characteristics, with special care for physical consistency in the non-linear regime. A two-tier cold/hot-FET procedure has been used, with the aim of improving the accuracy and speed of extraction. A comparison between measured and modelled S-

parameters at the operating point with V_{gs} = -2.5 V and V_{ds} = 8 V is shown in figure 4a, showing the accuracy of the results.

PRELIMINARY CIRCUIT DESIGN

MMIC circuit design employing the self-aligned gate technology has been undertaken, for demonstration of performance capabilities. A linear three-stage amplifier and a power stage have been designed in X band, and are currently being processed within the same wafer. The linear gain and input and output match of the linear amplifier are shown in figure 4b and 4c, where the Monte Carlo analysis includes process parameter tolerances. In figure 4d a picture of the power stage is shown, just prior to backside processing.

CONCLUSIONS

Self-aligned gate technology for high performance mono and multi-functional components has been demonstrated. Devices have been fabricated with good structural characteristics and performances; application to practical circuits is under way.

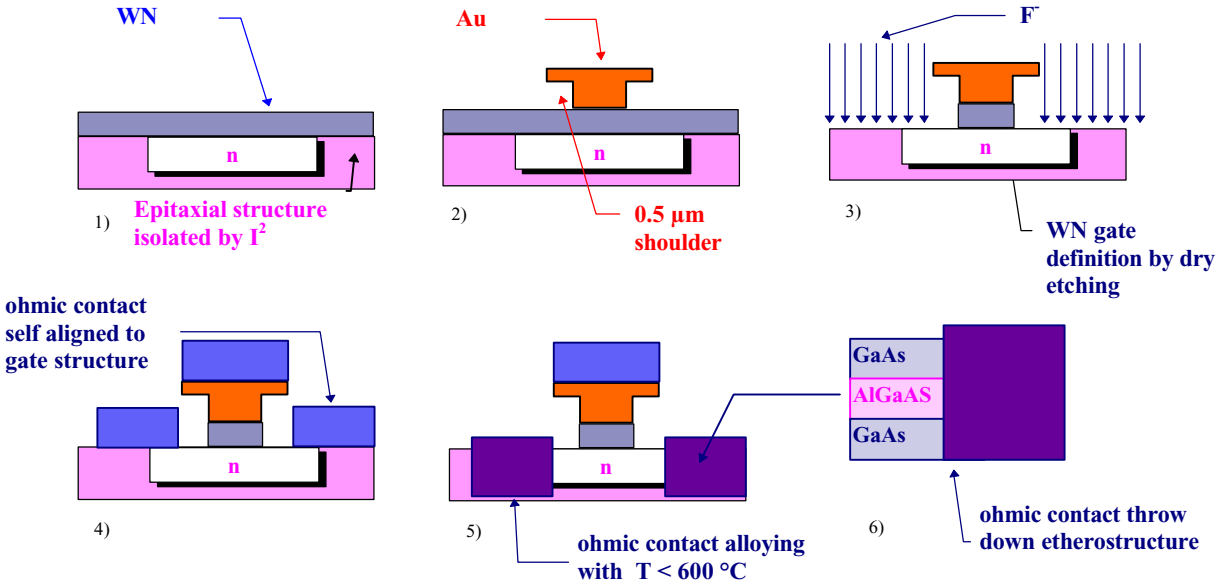
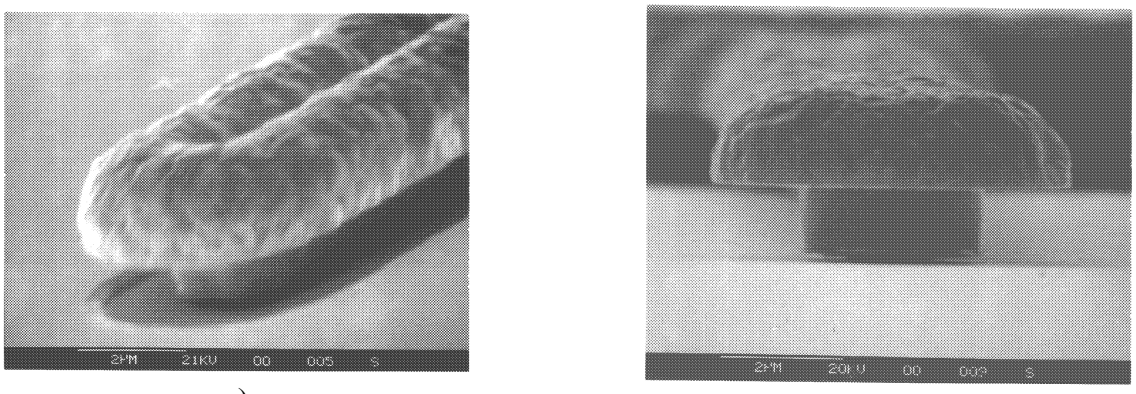


Figure 1 - 1) Isolation and WN reactive sputtering deposition; 2) Selective gold plating; 3) Schottky contact definition by selective CF_4 plasma etch; 4) Self align ohmic electrode formation; 5) Ohmic contact alloying process; 6) Ohmic contact penetration across epi layer



a) b)

Figure 2 - Plated gold/WN gate structure utilised for self-aligned ohmic contact fabrication

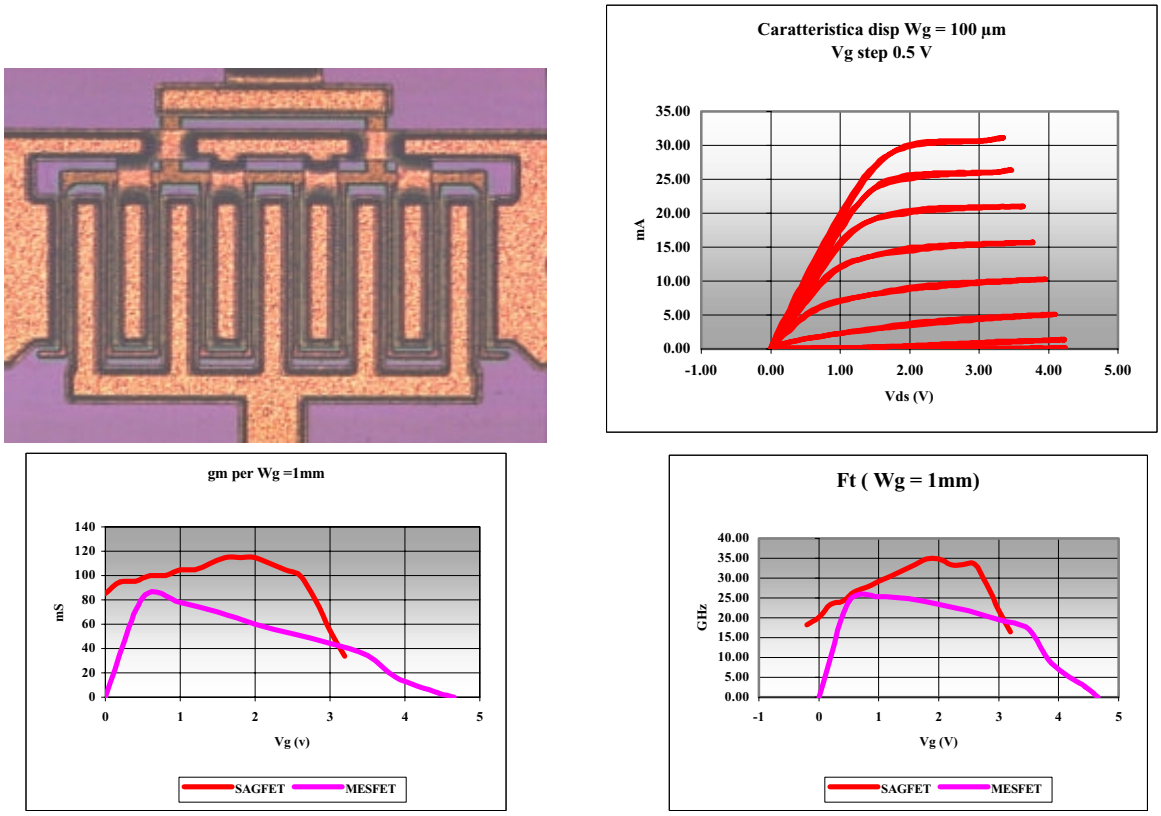


Figure 3 - DC Results obtained for epitaxial SAGFET: a) Device geometry; b) Device characteristic; c) Device transconductance and d) Device Ft as compared with MESFET devices

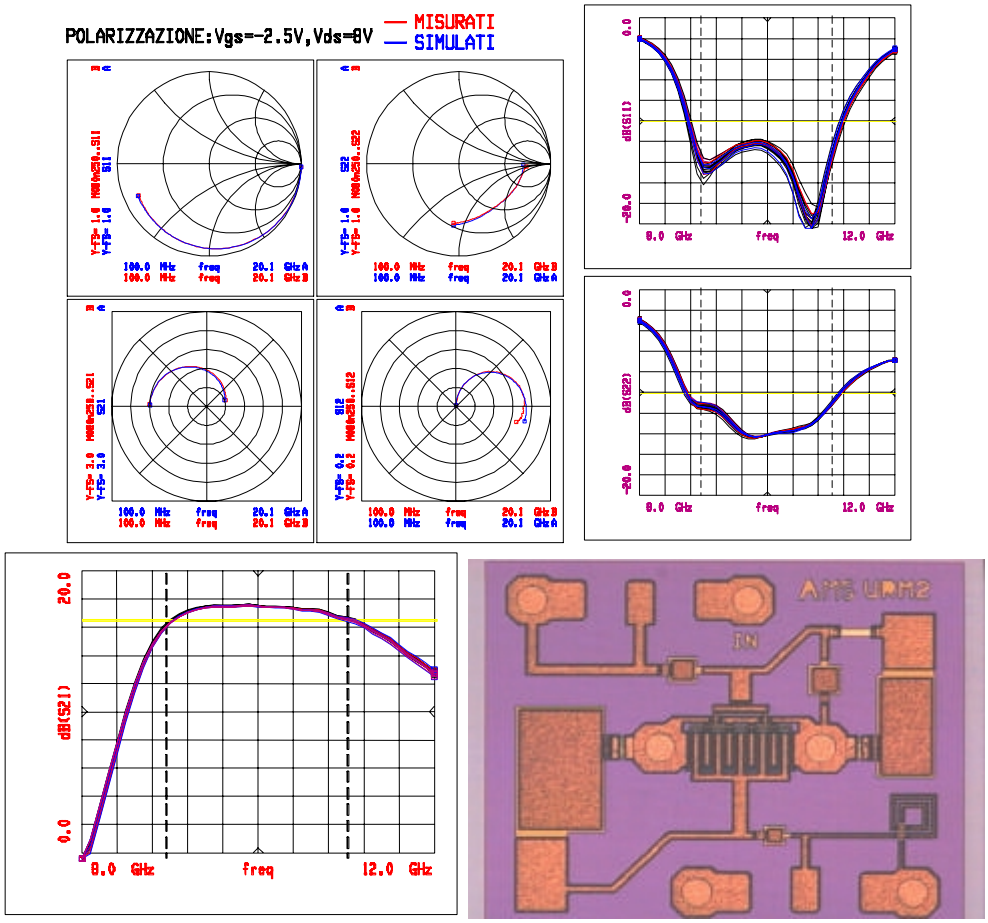


Figure 4 – a) Measured and modelled S-parameters of the SAGFET at V_{gs} = -2.5 V and V_{ds} = 8 V, b) designed input and output match of the linear amplifier (Monte Carlo analysis including fabrication tolerances), c) designed gain of the linear amplifier in X-band, d) photograph of the 1W power stage in X band