TRACKING SIC FET DEVELOPMENTS WITH A FET SIMULATOR

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ABSTRACT
SiC FETs promise high voltage working, high output power and a high impedance level for easy matching in applications at low gigahertz frequencies. RF SiC FETs development has been supported by practical investigation of dispersion using a pulsed *I(V)* measurement system, and by relating the multi-bias *S*-parameter behaviour of the devices to their material and structural features using a FET simulator. The simulator has been evolved through application in the GaAs industry. Modelling dispersion in all technologies is problematic because, whereas the origin of dispersion can be identified experimentally, the mechanism is not known in enough detail to include other than a generic model of it in the simulator. Nonetheless, the simulator is useful for interpreting practical device behaviour and for examining the likely performance benefits of any proposed changes to SiC FET structure.

INTRODUCTION
Wide bandgap materials with high breakdown field are attractive for high power RF applications where the supply voltage and dc power consumption are not limited by having to use batteries, as in portable applications. Such uses include radar, and radio network base stations. The attractions include high power for a given size of device and easy matching at power levels typical in these applications - attractions which remain despite low drift mobility with consequent high threshold field and voltage for full current to be attained. If the technology is to find its way into base stations and similar applications requiring linear power amplification, the problem to be solved (as in all semiconductor technologies) is dispersion, which is a memory effect that frustrates intelligent bias control schemes used to try and achieve circuit linearity from an inherently non-linear device.

A ROLE FOR A FET SIMULATOR IN SiC FET DEVELOPMENT
Depending upon one's ambition and experience with FET simulators in device development, roles varying from using a simulator as the main basis of technology development to using it in a monitoring and checking role are possible. Heavy reliance on a simulator is practicable when the task is to modify or improve existing device designs in a mature technology, for instance GaAs, where there are unlikely to be any nasty surprises in the form of unanticipated physical processes that have not been included in the simulator. Literally, it can take years to achieve agreement between measured RF behaviour and the simulator's predictions, all the while learning what processes and values the simulator needs to have included [1]. An important part of that effort is learning how to establish exactly what the technological make-up of the devices is. In a new technology, like SiC, the material and process control is insufficiently refined for predictions to be really close to practice, and there is wide variation in the devices' practical dc and RF behaviour anyway. The only realistic role for a simulator then is one of monitoring and checking, and using it to establish some likely broad trends in electrical behaviour resulting from gross technological changes.

DISPERSION
Dispersion is the term used to describe the fact that the dynamic *I(V)* and *C(V)* characteristics of devices are different from their static (or dc) characteristics. The time required for the dynamic (or instantaneous) set of characteristics to decay to the static set can range from a few tens of nanoseconds (in some GaAs devices) to hundreds of seconds for some SiC processes. Figure 1 shows the dynamic and static *I(V)* characteristics of a SiC FET measured with the pulsed-measurement instrument described in [2]. A reasonable first objective sufficient for some (but not all) practical applications of SiC FETs is to reduce dispersion to a level comparable with that found in ion-implanted FET foundry practice - an objective met by Figure 1.

Modelling dispersion is problematic in all technologies because, although the origin of dispersion can be located in general terms experimentally, the mechanism is not known in enough detail to include it in the simulator. GaAs technology is sufficiently mature to have eliminated dispersion from some types of device structure, but SiC FET

technology is too new to have achieved dispersionless behaviour reliably. Enough is known about how the processes responsible for dispersion affect the operation of a FET *generically* to be able to include it in the simulator as a transform, involving only two unknown variables, which connects the dynamic to the static characteristics. Fundamentally, with fixed deep-level charge and fixed lattice temperature, a simulator calculates a set of RF (i.e. dynamic) characteristics, from which the dc characteristics can then be obtained via the transform. The trouble is that the values of the two transform variables have to be found from experience with the particular technology: they are not available *a priori*, which severely restricts the predictive capacity of the simulator as a technology development aid.

BACKGROUND TO THE SIMULATOR

The FET simulator used in this work is a simplified version of a HEMT simulator developed around what we call the macrocell approach [3]. A mesh of coarse, interlocking, cells is used instead of the commonplace fine mesh. The mesh configuration is so chosen that, within each cell, one physical process predominates. A fully two-dimensional solution is found by adjusting the cell sizes to minimize the error in satisfying boundary conditions of electric flux and current continuity across all cells. In principle the simulator caters for HEMT and FET structures constructed in various elemental and compounds, but the problem always is one of obtaining the materials and carrier transport data the simulator requires. The difficulty escalates dramatically in going from a relatively simple single-host-material device like a GaAs FET to a pseudomorphic heterojunction system.

One of the unforeseen lessons in using such a simulator for yield prediction of complete MMICs is the high precision with which the technological data input to the simulator must be known [1].

To gauge the general effectiveness of the simulator, Figure 2a shows the form of the gate-channel capacitance extracted for a PHEMT from multi-bias *S*-parameter measurements, while Figure 2b shows the output of the simulator for a similar structure. The practical form is unlike that commonly seen in GaAs FETs where the capacitance goes on increasing as V_{GS} is made more positive; in the PHEMT the capacitance at first increases but then decreases. The simulator has produced the same form. Figure 3a shows the measured *I(V)* characteristics of the same type of device; there is negative differential conductivity which is reproduced by the simulator (Figure 3b).

APPLICATION TO SIC FETs

A realistic role for the simulator is to predict broad trends in device behaviour that might follow from gross changes in the make-up of the device, such as doubling the channel doping density, using a markedly different doping profile, a different recess depth and offset, or a different gate length. To illustrate the possibilities, an example will be given of the likely effect of reducing the gate length on the 1GHz behaviour. The results apply to a nominal 0.8μm gate FET with a 0.4μm channel doped to low-to-mid $10^{17}cm^{-3}$.

Figure 4a shows the predicted dc characteristics for the nominal device while Figure 4b shows the RF characteristics for bias at V_{DS} = 25V.

Figure 5 shows the predicted MAG for this particular structure as the gate length is decreased. Surprisingly perhaps, at least at first sight, the gain decreases. The reason is to be found in Figures 7 and 8.

Figure 6 shows what happens to the dc drain current for various gate voltages at a drain bias of 40V. The drain current increases as the gate length is decreased owing to the potential drop in the leading edge of the depletion region, starting from the source-edge of the gate and extending down the channel, decreasing. A smaller potential drop in the leading edge of the depletion region means the depth of depletion decreases, so the channel opening at the minimum point is larger, and hence the drain current is larger. The absolute value of the drain current, however, is far less important to the gain than the *incremental* change in the current per unit change in gate voltage, i.e. g_{m0}.

Figure 7 shows the transconductance, g_{m0}. In this device, as the gate length is decreased, g_{m0} drops despite the fact that the depth of depletion decreases. One-dimensional theories cannot accommodate these two outcomes: the reason is entirely two-dimensional. When the gate voltage is changed incrementally, the charge on the gate changes incrementally, and what is important is where the field associated with this charge change ends up. At the larger gate lengths, much of the field terminates in the lower edge of the depletion region and so is effective in modulating the channel opening. As the gate is made progressively shorter, an increasing fraction of the field arising from the charge change is syphoned off into the depletion region extension in the gate-drain space and so is not effective in modulating the lower edge of the depletion region.

Figure 8 shows what happens to the drain-source resistance, R_{ds}, as the gate length is decreased. R_{ds} decreases, a change

which also serves to reduce the gain.

The guideline which emerges from such simulations is that for there to be any benefit in going to shorter gate lengths the channel thickness needs to be decreased, so L_G/W is larger. The channel doping needs to be increased correspondingly to carry the same drain current.

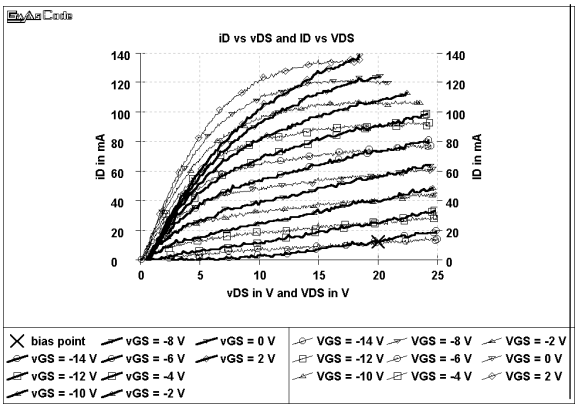

Fig. 1: Dynamic (thick lines) and static (thin lines) characteristics of a SiC FET.

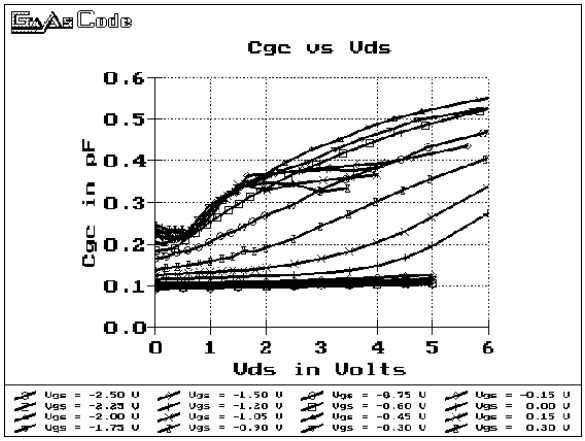

Fig. 2a: Form of gate channel capacitance of a PHEMT extracted from measured *S*-parameters.

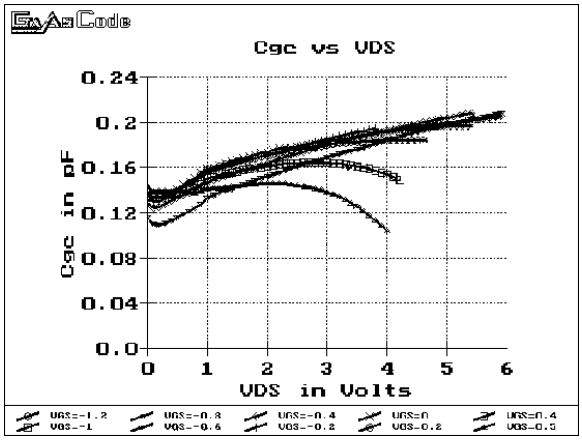

Fig. 2b: Form of gate channel capacitance of a similar type of device to figure 2a produced by the simulator.

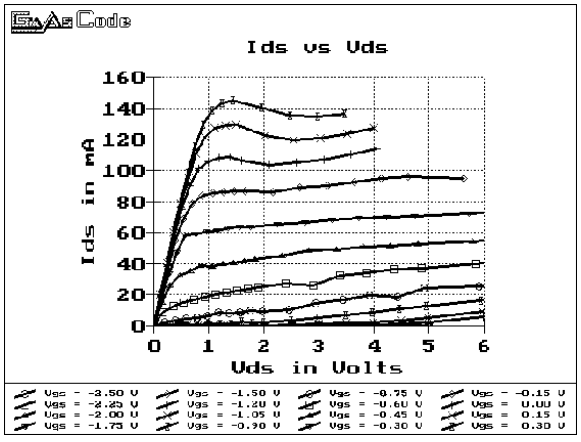

Fig. 3a: Form of *I(V)* characteristics for a PHEMT extracted from measured *S*-parameters.

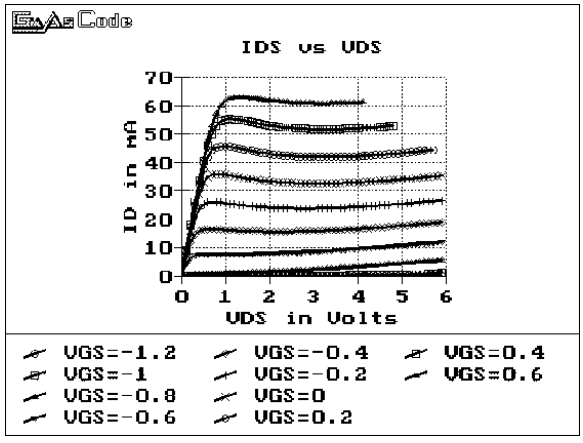

Fig. 3b: Form of *I(V)* characteristics for a similar type of device as 3a produced by the simulator (gate width differs).

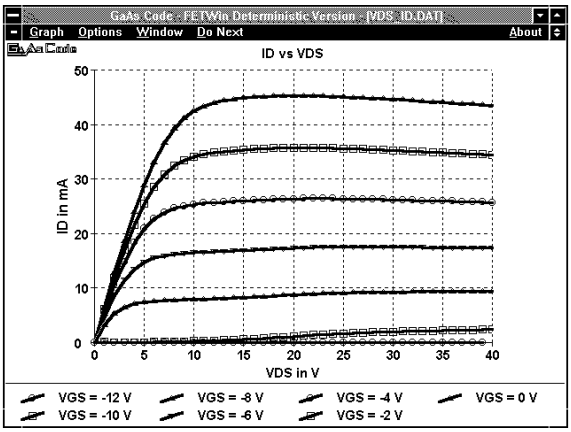

Fig. 4a: Predicted dc characteristics for SiC FET with nominal gate length of 0.8μm.

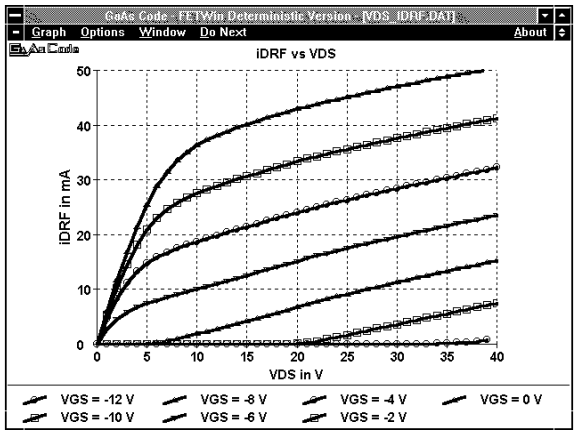

Fig. 4b: Predicted RF characteristics for the device of figure 4a biased at V_{DS} = 25V.

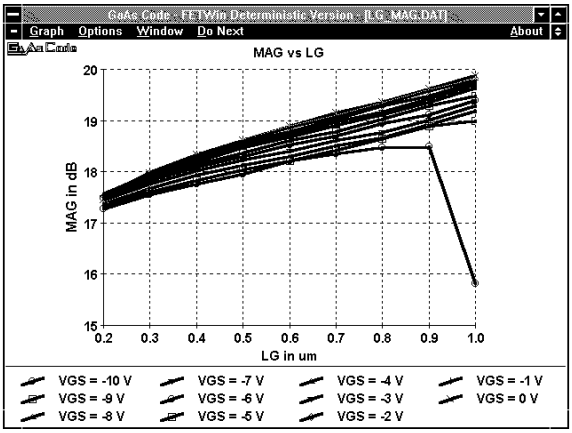

Fig. 5: Variation in predicted gain (MAG) as gate length is varied in the simulator.

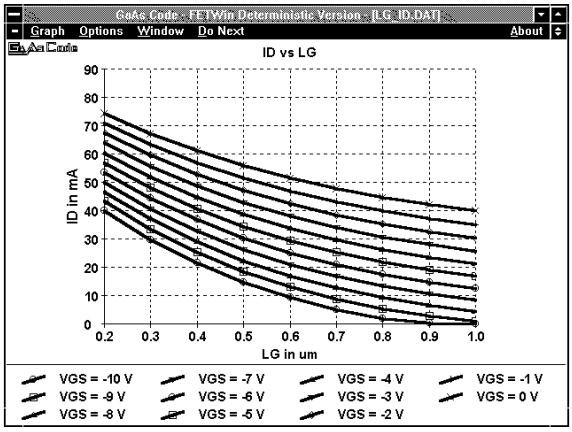

Fig. 6: Variation in dc drain current as gate length is varied in the simulator.

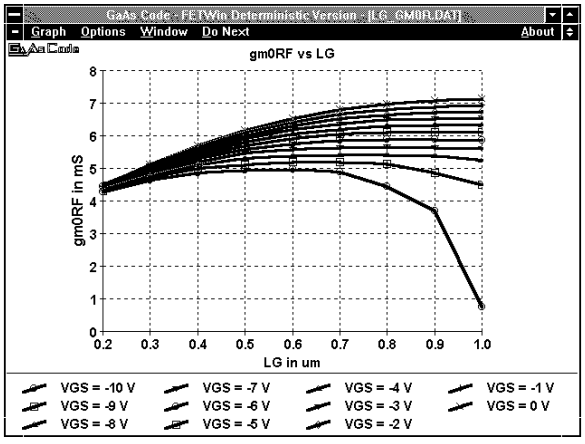

Fig. 7: Variation in predicted RF transconductance as gate length is varied in the simulator.

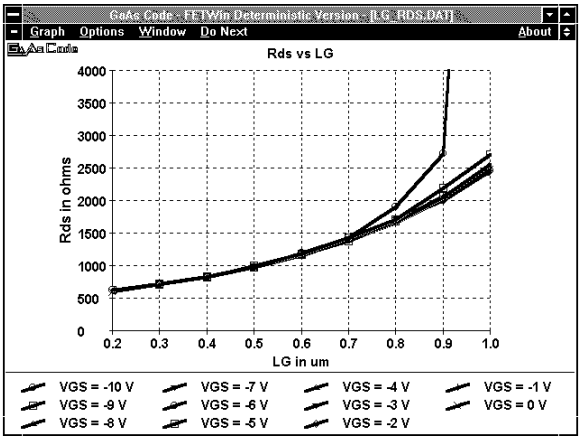

Fig. 8: Variation in predicted value of output resistance as gate length is varied in the simulator.

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