Ultra-short T-shaped gate fabrication technique for InP based HEMTs with high f_t (> 300 GHz) and their MMIC applications

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ABSTRACT

A fabrication technique for sub-50-nm T-shaped-gate InGaAs/InAlAs high electron mobility transistors (HEMTs) lattice-matched to InP substrates and their device characteristics are presented. A 35-nm T-shaped-gate HEMT is successfully fabricated by optimizing conditions of electron beam (EB) lithography and reactive ion etching (RIE) to make an ultra-fine resist pattern and precisely replicate it on a SiO_2 film, which defines gate length (L_g). The device exhibits an excellent current-gain cutoff frequency (f_T) as high as 317 GHz with high controllability. This technique is considered to be very effective for device and MMIC applications in the V band and even higher frequency ranges.

INTRODUCTION

InP-based InGaAs/InAlAs high electron mobility transistors (HEMTs) are considered to be one of the most promising devices for millimeter-wave and optical communications because of their superior high-frequency and low-noise performances. This is due to high electron mobility, high saturation velocity, and high sheet carrier density obtained in this system. A shorter gate is also essential for the ultra-high RF performance. In fact, RF performances have been significantly improved by reducing gate length (L_g) down to 50 nm or below [1, 2, 3]. These short gates were fabricated with T-shaped geometry to reduce gate capacitance as well as gate resistance. As for sub-50-nm-gate HEMTs, Suemitsu *et al*. reported an excellent RF performance in a 30-nm T-shaped gate HEMT [2]. However, the gate-head of the T-shaped gate directly touched the dielectric film deposited on epitaxial layers, which might increase parasitic fringe capacitance. Wakita *et al*. proposed a trilayer resist process for sub-0.1-µm T-shaped gate fabrication [4], in which the gate-head is separated from the dielectric film.

In this paper, we have developed a sub-50-nm T-shaped-gate fabrication technique using a conventional trilayer resist system by optimizing EB lithography and RIE conditions, demonstrating f_T of over 300 GHz in a 35-nm-gate HEMT.

FABRICATION PROCESS

The HEMT epitaxial layers consists of an InAlAs buffer layer (300 nm), an InGaAs channel layer (15 nm), an InAlAs spacer layer (3 nm), Si planar doping (5×10^{12} cm^{-2}), an InAlAs barrier layer (10 nm), an InP etch-stopper layer (6 nm), and a Si-doped InGaAs cap layer (25 nm), which were grown on a semi-insulating (100) InP substrate by metalorganic chemical vapor deposition (MOCVD). The electron mobility of the two-dimensional electron gas is 8100 cm^2/Vs and the sheet carrier density is 2.6×10^{12} cm^{-2} at room temperature, which was measured after the n^+-InGaAs cap layer was removed down to the InP etch-stopper layer by wet chemical etching.

Mesa structures were formed by photolithography and wet chemical etching. The InGaAs channel layer was selectively recessed using an aqueous solution of citric acid ($C_6H_8O_7$) and hydrogen peroxide (H_2O_2) mixture to form air gaps between the gate metal and the InGaAs channel [5]. Source and drain ohmic contacts were formed using alloyed AuGe/Ni/Au at 270°C for 10 minutes in a nitrogen atmosphere, and the separation between source and drain electrode pads was 2 µm. The measured contact resistance was typically 0.066 Ω mm. A 25-nm-thick SiO_2 film, which improves resist adhesion, defines the gate footprint and mechanically supports the T-shaped gate, was evaporated at a substrate temperature of below 120°C.

In order to fabricate sub-50-nm T-shaped-gates, conditions of electron beam (EB) lithography were optimized to make an ultra-fine pattern below 50 nm. EB exposure was carried out with a beam current of 100 pA using a 50-keV JEOL EB machine. Figure 1 shows line dose dependence of pattern size of a single ZEP layer when developed in a methyl isobutyl ketone (MIBK) / isopropyl alcohol (IPA) solution. The

pattern size was precisely controlled from 15 nm to 40 nm using a single line exposure with a dose from 1.0 nC/cm to 11.3 nC/cm. A trilayer EB resist, that consists of a bottom ZEP layer, a middle PMGI layer and a top ZEP layer, was then coated on the SiO_2 film. The top layer, which was developed in a high sensitive solution of methyl ethyl ketone (MEK) / methyl isobutyl ketone (MIBK), was exposed with a relatively low area dose of 70 $\mu C/cm^2$ so as not to affect the bottom layer. The bottom layer was exposed with a line dose of 8 nC/cm and developed in a low sensitive MIBK/IPA solution. Figure 2(a) shows a cross-sectional scanning electron microscope (SEM) image of the trilayer just after EB lithography. The fine gate-foot pattern could be fabricated with an overhang structure for the gate-head.

Reactive ion etching (RIE) conditions to precisely replicate the fine resist patterns on the SiO_2 film were also optimized. It should be noted that the EB resist itself is also etched during the RIE process, therefore, the etching conditions must be chosen by taking account not only of replicated SiO_2 opening size but also of remaining resist thickness after RIE. Two etching gases, CF_4 and CHF_3, were then tested. It is well known that etching rate ratio of SiO_2/resist can be increased by using CHF_3 due to a formation of crosslinked polymers only on the resist surface, which act as etching barriers for the resist. In fact, the etching rate of the resist was found to be 20 nm/min, which was 80% smaller than that (104 nm/min) for CF_4, and the etching rate ratio to be 1.17 [cf. 0.35 for CF_4]. Figure 3 shows pattern size dependence of the etching rate of SiO_2 for CF_4 (30 sccm, 4.0 Pa, 100 W, 90 sec) and CHF_3 (15 sccm, 2.0 Pa, 100W, 90 sec). It is notable that the etching rate for CHF_3 decreased rapidly down to zero when the pattern size became below 40 nm, while that for CF_4 decreased slowly. This phenomenon is considered to result from the formation of polymers even on the sidewalls of the resist pattern, which blocked SiO_2 etching when the pattern size was so small as to be closed by the polymers. Therefore, the polymer size was estimated to be about 20 nm, which equals to half of the pattern size of 40 nm.

Figure 4 shows cross-sectional SEM images of the fine resist pattern on a 25-nm-thick SiO_2 film before (inset) and after RIE process and the following recess etching for CF_4 (1 min) and CHF_3 (4 min). The SiO_2 opening sizes as a function of the pattern size are plotted in Fig. 5. Slightly increased openings compared to the pattern size could be realized and the ultra-fine pattern as small as 15 nm could be clearly replicated on the SiO_2 film with CF_4. Furthermore, the surface of the remaining resist was very smooth. On the other hand, the SiO_2 opening size was much decreased with CHF_3 despite the etching time was extended to 4 minutes, and the surface of the resist was rough due to the formation of the polymers. The remaining resist thickness was about 90 nm, which defines the height of the gate-foot of a T-shaped gate. Controllability was thus much improved using CF_4, and this technique enabled precise control of L_g even in the sub-50 nm region with keeping the remaining resist thick enough and its surface smooth. Using this condition, the fine resist pattern was successfully replicated on the SiO_2 film as shown in Fig. 2(b).

After the RIE process, wet chemical etching using an aqueous solution of $C_6H_8O_7$ and H_2O_2 mixture formed the gate recess in the n^+-InGaAs cap layer. Ti/Pt/Au gate metal was finally evaporated and lifted off. The temperature throughout the whole process was kept below 270°C to prevent electrical degradation caused by thermally diffused fluorine atoms [6, 7]. Figure 6 shows a cross-sectional transmission electron microscope (TEM) image of a fabricated T-shaped-gate. An ultra-short T-shaped gate as short as 35 nm was thus successfully fabricated.

DEVICE CHARACTERIZATION

Figure 7 shows the typical current-voltage (*I-V*) characteristics of the fabricated 35-nm-gate HEMT. The device is well pinched off, and the maximum DC transconductance (g_m) of about 1.0 S/mm was achieved. Precision S-parameter measurements were carried out in a frequency range from 0.25 to 50 GHz using a vector network analyzer (HP8510C) in on-wafer configuration. S-parameters for open pad on the same wafer were also measured to calibrate the parasitic capacitance components related to the pad metals. Figure 8 shows the frequency dependence of current gain ($|h_{21}|^2$) of the device when biased at a drain-source voltage (V_{DS}) of 1.0 V and a gate-source voltage (V_{GS}) of -0.6 V. The current-gain cutoff frequency (f_T) was deduced as high as 317 GHz by extrapolating $|h_{21}|^2$ with a -20 dB/decade slope. The cutoff frequency exceeds 300 GHz in a range of V_{GS} = -0.8 V to -0.5 V (V_{DS} = 1.0 V) as shown in Fig. 9.

CONCLUSION

We developed an ultra-short T-shaped gate fabrication technique for InGaAs/InAlAs HEMTs by optimizing EB lithography and RIE conditions, which enables us to make an ultra-fine resist pattern as small as 15 nm and precisely replicate it on a SiO_2 film. A fabricated 35-nm-gate HEMT showed excellent f_T as high as 317 GHz. This technique is considered to be very attractive for device and MMIC applications at 60 GHz, 77 GHz, and even higher frequencies.

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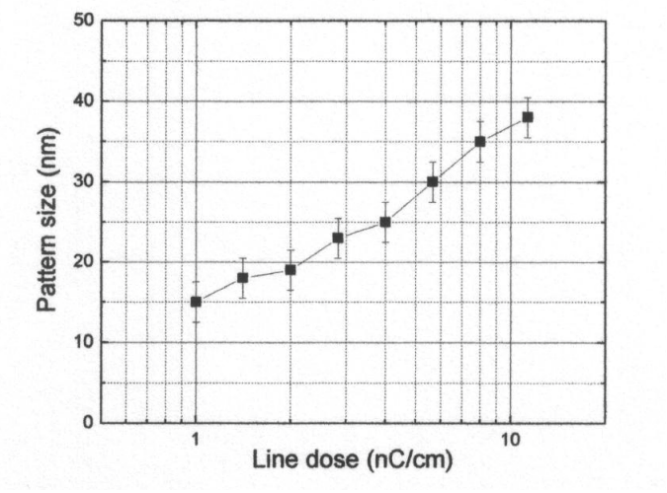

Fig. 1. Resist pattern size of a single ZEP layer vs. line dose.

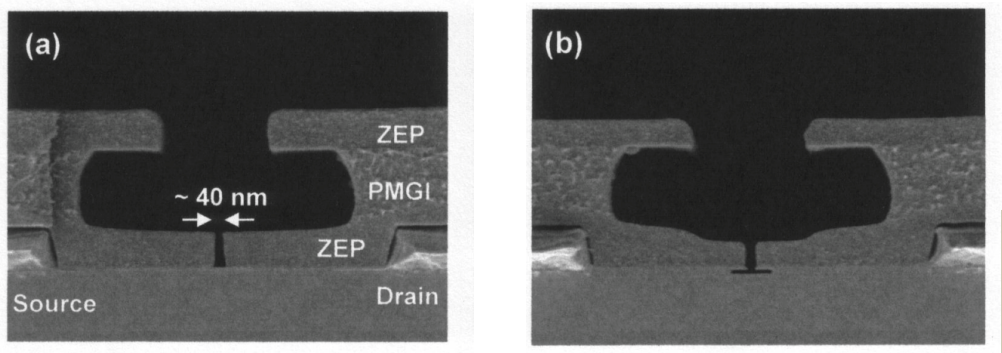

Fig. 2. Cross-sectional SEM images of the trilayer after (a) EB lithography and (b) RIE using CF_4 for 1 mm.

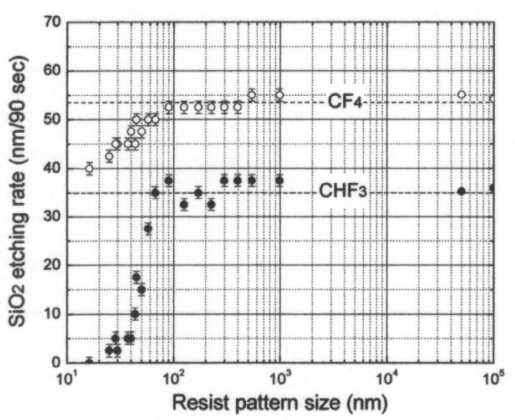

Fig. 3. Resist pattern size dependence of SiO_2 etching rate for CF_4 (open circles : 30 sccm, 4.0 Pa, 100 W, 90 sec) and CHF_3 (solid circles : 15 sccm, 2.0 Pa, 100 W, 90 sec).

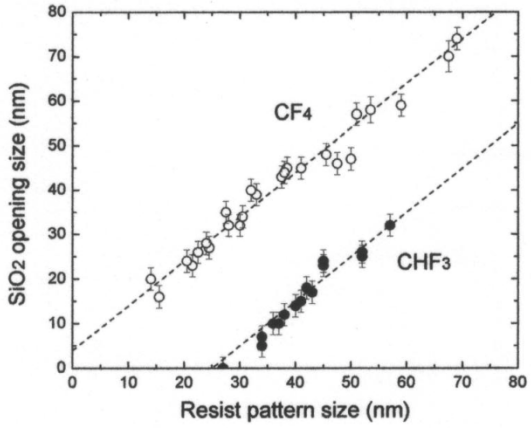

Fig. 5. SiO_2 opening size vs. resist pattern size for CF., (open circles : 30 sccm, 4.0 Pa,100 W, 1 min) and CHF_3 (solid circles : 15 sccm, 2.0 Pa, 100 W, 4 min).

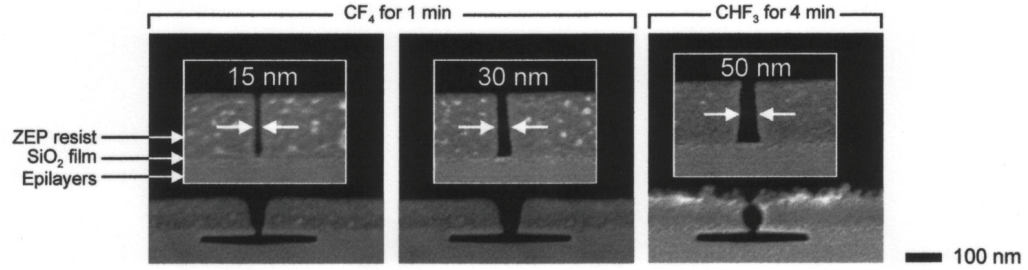

Fig. 4. Cross-sectional SEM images of the tine resist pattern on a 25-nm-thick SiO_2 film before (inset) and after RIE and the following recess etching for CF_4 and CHF_3.

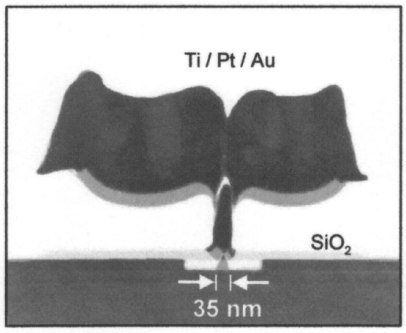

Fig. 6. Cross sectional TEM image of a 35-nm-T-shaped gate.

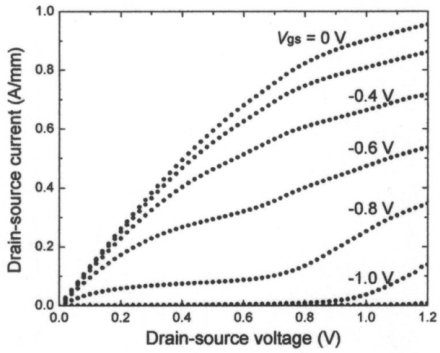

Fig. 7. Typical I-V characteristics of a 35-nm-gate HEMT. The gate-source voltage (V_{GS}) is changed from 0 V to -1.2 V in -0.2Vsteps.

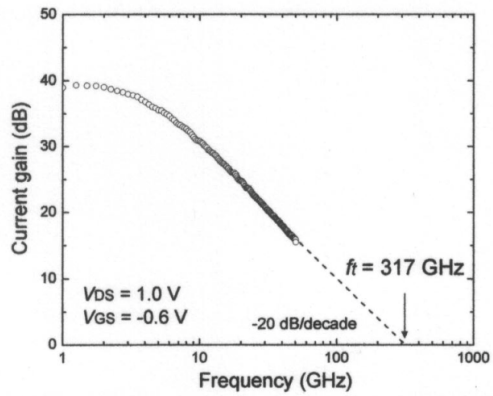

Fig. 8. Frequency dependence of current gain $|h_{21}|^2$ for the 35-nm-gate HEMT biased at a drain-source voltage V_{DS} = 1.0 V and a gate-source voltage V_{GS} = -0.6 V.

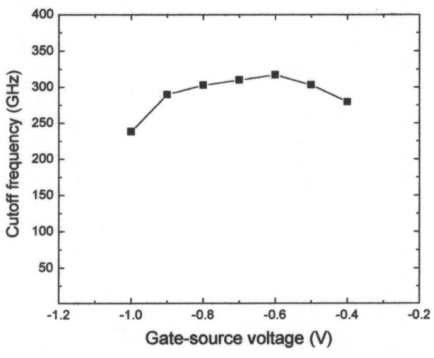

Fig. 9. Gate-source voltage V_{GS} dependence of cutoff frequency f_T for the 35-nm-gate HEMT biased at a drain-source voltage V_{DS} = 1.0V.