DESIGN OF COPLANAR POWER AMPLIFIERS FOR MM-WAVE SYSTEM APPLICATIONS INCLUDING THERMAL ASPECTS

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ABSTRACT

Due to the poor thermal conductivity of GaAs, successful power amplifier design in coplanar technology requires careful thermal considerations. The influences of the active device geometry and mounting conditions have been investigated theoretically and experimentally to provide reliable thermal management design data. 50-µm thinning and flip-chip with thermal bump attachment on AlN or diamond exhibited temperature rises in the order of 50 and 40-30 °C respectively, leading to significant improvement in the performance of coplanar power devices and circuits. These results demonstrate the potential of coplanar MMIC technology for high power applications.

I. INTRODUCTION

For three years, the market of wireless communication systems operating in the 20 to 60 GHz frequency range has exploded. To provide subscribers with communication services such as telephone, video and Internet, satellite links and multipoint distribution services (LMDS and MVDS) are being implemented at *Ka*-, *Q*-, and *V*-band. These commercial applications have created a demand of watt-level GaAs power amplifiers (PA). In contrast to microstrip amplifiers that have demonstrated high output power with good thermal properties (e.g. [1]), the coplanar (CPW) technology did not receive up to now any interest in power applications. This results from the poor power handling capabilities of CPW and the absence of via-holes and backside process usually contributing significantly to heat removal in microstrip circuits. However, due to its technical and technological advantages, the coplanar GaAs MMICs have demonstrated to be cost effective for volume production [2]. Besides, with the emerging mounting solutions like the flip-chip (FC) technique, nowadays the thermal limitations of CPW can be overcome.

In this paper, based on rigorous numerical analyses and measurements, we discuss the design issues in the thermal management of CPW MMIC power amplifiers, such as transistor geometry, chip size and different mounting conditions, from device to circuit level. All the coplanar MMICs presented here were designed and fabricated at the FhG-IAF using our double δ-doped AlGaAs/InGaAs/GaAs PHEMT process with 0.15-µm T-gates on 3" and 4" wafers [3]. A rigorous design methodology including thermal considerations is the key to achieve the range of output power and reliability for the coplanar MMIC amplifiers reported in Table I.

TABLE I. EXAMPLES OF MILLIMETER-WAVE COPLANAR POWER AMPLIFIERS REALIZED AT THE FRAUNHOFER-IAF.

Frequency [GHz]	Gain [dB]	P_{-1dB} [dBm]	P_{sat} [dBm]	PAE_{max}	Chip size [mm²]
25-27	17	26-27	28	20	7.5
28	14	27	29	17	6.0
35	14	27	28	12	2.6
35	9.5	28.6	30.1	12	7.5
36-40	10	24	26	7	4.0
42	12	26	27	15	2.6
60	9.5	24	25	14	4.5

II. THERMAL CONSIDERATIONS IN COPLANAR MMIC DESIGN

As illustrated in Fig. 1, the intrinsic device performance, like the transconductance G_m and the drain current I_d are strongly dependent on the device temperature. In coplanar technology, the FET temperature profile depends considerably on the device geometry (gate-to-gate spacing, source island interconnect, etc.) and the mounting conditions (on-wafer or single-chip die, chip thickness, conventional face-up or flip-chip attachment to a heat sink, [4]). In Fig. 2, one sees that different gate-to-gate spacings (or "gate pitch") lead to significant temperature rises at the FET level for a chip soldered to a copper carrier on chuck. However, if the larger gate pitch reduces heating, in order to minimize the device parasitics, pitches below 30 µm should be used for millimeter-wave applications. The Fig. 2 shows that in conventional face-up (conv. FU) mounting, the substrate thickness plays a major role as well; thinning a chip to 100 µm contributes directly to a lower thermal resistance, and thus a better operating temperature with respect to the dissipated power.

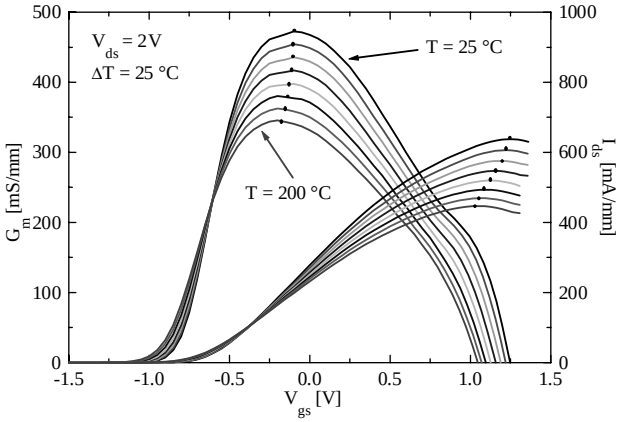

Fig. 1: Measured transconductance and drain current of a 6×100 µm PHEMT as a function of the gate-source voltage, for different thermal-chuck temperatures (25 °C to 200 °C in step of 25 °C).

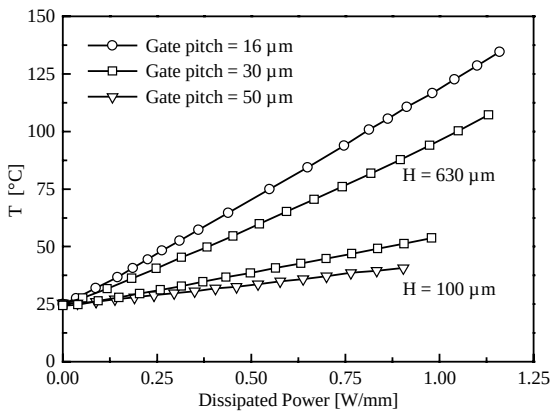

Fig. 2: Measured temperature for a single chip 7×100 µm PHEMT mounted on copper/chuck (size 0.7×0.45 mm²) as a function of the dissipated output power and chip thickness (635 µm and 100 µm), T_{amb}=25 °C.

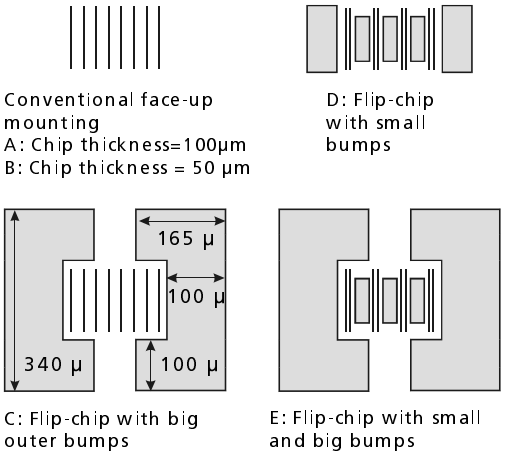

Fig. 3: Different possible layouts and bump configurations for a millimeter-wave power PHEMT (8×75 µm). Inner source island thermal bump = 20×60 mm².

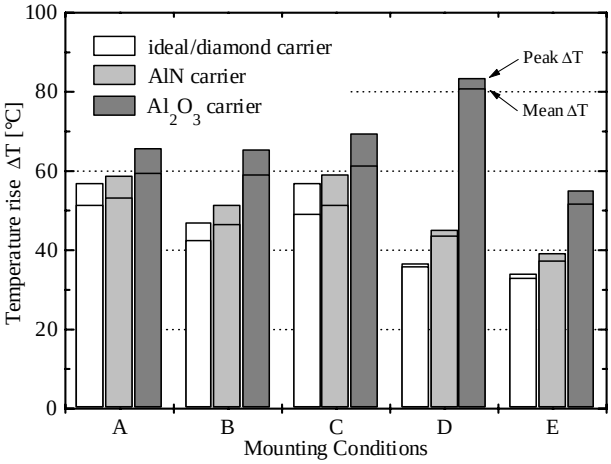

Fig. 4: Simulated temperature increase (peak and mean) of 8×75 µm PHEMT, P_{diss}=1 W/mm, for different FET layouts and mounting conditions (cases A, B, C, D, E from Fig. 4).

TABLE II. MEASURED TEMPERATURE RISE OF 7×75 µM FETS (LAYOUT D, FIG.4), P_{DISS}=1W/MM, FOR DIFFERENT MOUNTING CONDITIONS. CARRIER SIZES: CONV. /ALN= 25×25×0.63 MM³, FC/ALN= 10×10×0.63 MM³, FC/DIAMOND= 5.5×5.5×0.3 MM³ [5].

Type	GaAs HEMT layout	GaAs chip volume	Mounting conditions	Temperature rise ΔT
Conventional Face up	Mmw-FET layout D Without bumps	12 × 12 × 0.635 mm³	Chuck (≡on-wafer meas.)	45 °C (→ 70 °C)
		12 × 12 × 0.635 mm³	Epoxy/AlN/Chuck	41 °C (→ 66 °C)
Flip-chip on AlN	Mmw-FET layout D With 5 gold bumps	1 × 2 × 0.635 mm³	AlN/Chuck	19 °C (→ 44 °C)
		1 × 2 × 0.635 mm³	AlN/Epoxy/Cu/Chuck	18 °C (→ 43 °C)
Flip-chip on diamond	Mmw-FET layout D With 5 gold bumps	1 × 2 × 0.635 mm³	Diamond/Chuck	16 °C (→ 41 °C)
		1 × 2 × 0.635 mm³	Diam./Epox./Cu/Chuck	13 °C (→ 38 °C)

For the 8×75 µm FETs in a single die form (2×2 mm²) of Fig. 3, the simulated temperature rises ΔT for different layouts and mounting conditions are illustrated on Fig. 4. Compared to a 635-µm thick diced FET in conv. FU mounting (ΔT>>100 °C, Fig. 2), the 100-µm or 50-µm thinning (cases A, B) lower the temperature rises to already 58 °C and 50 °C respectively, for an attachment on aluminum nitride (AlN, λ=180 W/mK), whereas the use of alumina is less effective (λ_{Al2O3}=30 W/mK). In flip-chip mounting, the thermal management realized using two big gold bumps closely placed to the outer sources (case C) of an 8×75 µm FET is near to that a 100-µm thinning. However, much better heat dissipation is achieved using smaller bumps directly placed on the internal source islands (cases D and E), with temperature rises of only about 45 °C on AlN and below 40 °C on diamond (that is used as reference). The table II shows the measured temperature rise for different mounting conditions of an "8"×75 µm FET, when one finger is replaced by a temperature sensor [4]. Because very good agreement between measurements and simulations for 7 active fingers were achieved [5], it is possible to perform meaningful simulations under unchanged boundary conditions for 8 active fingers (i.e. Fig. 4). The extrapolated values when all the FET fingers are active, are given in parentheses in Table II; for similar mounting conditions, they agree well with those of Fig. 4 (e.g. case D, FC/AlN, and Table II, lines 3-4) and with the data published in [6]. The first line from Table II indicates that the *on-wafer* characterization of 635-µm thick wafers or large chips does not represent a *so bad* case; because the large lateral dimensions play a significant role in the heat dissipation. This confirms

the full 3-dimensional nature of the heat flow in coplanar waveguide ICs. As demonstrated by the measurements, the best results are those obtained with flip-chip on diamond (lines 5-6). However, acceptable thermal management ($\Delta T \approx 40$ °C) is also achieved using of a chip flipped with thermal gold bumps on AlN (lines 3-4, i.e. approximately equivalent to a 50-µm thinned chip placed on a heat sink). Furthermore, in comparison with chips only mounted or flipped on AlN, lower temperatures are achieved using AlN/Epoxy/Copper, which is due to an even better thermal attachment to the heat sink.

III. EXAMPLES OF MILLIMETER-WAVE COPLANAR MMIC AMPLIFIERS

In addition to rigorous layout design, the PA optimization is based on the load line approach considering general and loop stability, gain, bandwidth, and output power. The input, inter-stage and output matching networks have the task of transforming 50 Ω impedances from the RF ports to the very low impedances of the power devices. However, the coplanar technology faces the problem that the conventional characteristic impedance range is limited to approximately 30-70 Ω. In CPW, low impedance transmission lines were realized using multi-finger or capacitively loaded transmission lines [7]. For both, as well as for basic passive elements, broadband models have been derived from test-structures and validated up to and above W-band [8,9]. The two following examples illustrate the success of our global coplanar power amplifier design strategy.

A. Flip chip of 60 GHz medium power amplifier

For applications at 60 GHz, medium power amplifiers (MPA) using optimized 4 × 60 µm devices were designed and fabricated (Fig. 5). The temperature profiles of the FETs embedded in the MMIC were calculated by means of thermal simulations, on-wafer and flip-chip with or without thermal bumps. For the power levels and the devices considered here, two bumps placed close to each transistor improve significantly the temperature profile in flip-chip mounting. Fig. 6 shows the effects of the thermal bumps on the MPA performance. Mounting without thermal bumps leads to a significant reduction in both gain and output power, whereas with thermal bumps, the amplifiers reach the expected saturated output power of 200 mW at 60 GHz, with more than 10 dB linear gain and 21 % power-added-efficiency. In addition, due to the low parasitics of our optimized flip-chip interconnects, the small signal S parameters (Fig. 7) remain almost identical to those obtained on-wafer, resulting in a predictable amplifier behavior either on-wafer or in flip-chip package.

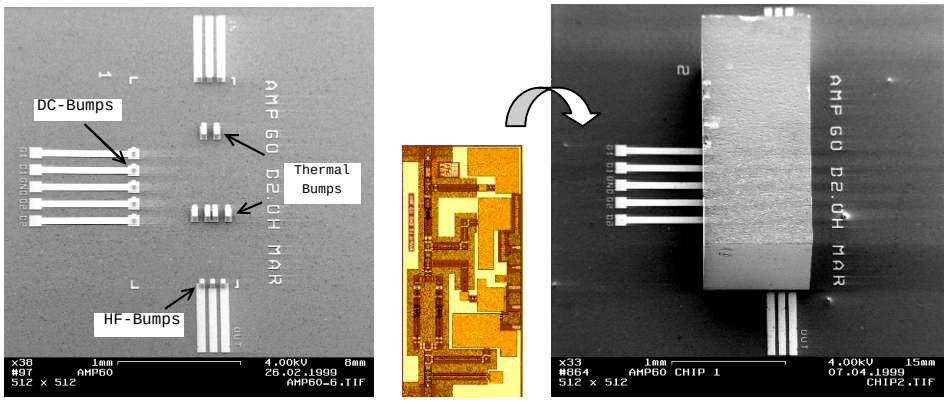

Fig. 5: SEM and chip photographs of the 60-GHz MPA (center, 1.0×2.0mm²), placement of RF, DC and thermal bumps (left, thermal bump size is 40×100µm²) and FC on AlN (right).

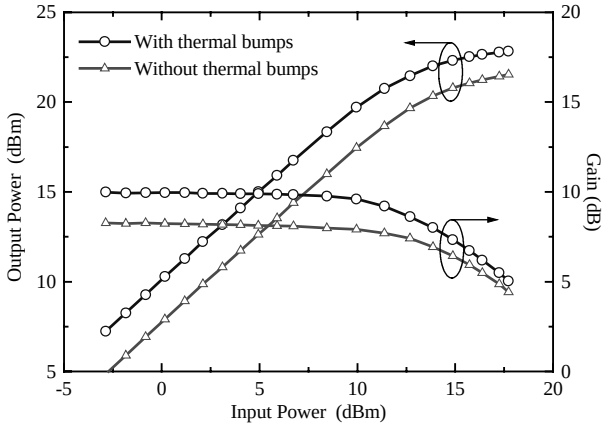

Fig. 6: Measured output power and gain of 60-GHz Flip-chip MPA with and without thermal bumps.

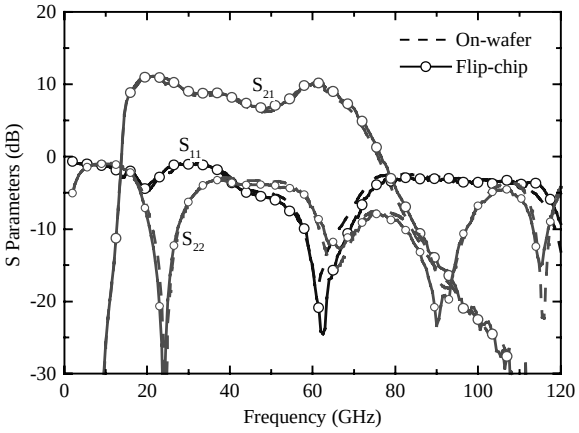

Fig. 7: Measured S parameters of the 60-GHz MPA on-wafer and after Flip-chip with thermal bumps.

B. High power Ka-band amplifier

To demonstrate the potential of the coplanar technology for high power applications at *Ka*-band, a compact (2.45 × 2.95 mm²) 2-stage high power amplifier (HPA) has been developed (Fig. 8). At 35 GHz, and at a drain voltage of 3.25 V, this HPA has demonstrated *on-wafer*, a linear gain of 9.5 dB and the highest output power ever reported at *Ka*-band for coplanar MMIC, namely a P_{-1dB} of 725 mW and more than 1 Watt of saturated output power as shown on Fig. 8. To verify the benefit of realistic mounting solutions (50-µm chip mounted or flipped with thermal bumps on a AlN carrier), an equivalent reduction of the temperature profile, performed using a thermally controlled chuck, demonstrated an increase in performance with a linear gain of 10.4 dB, P_{-1dB}=950 mW and P_{sat}=1.2 Watt [10].

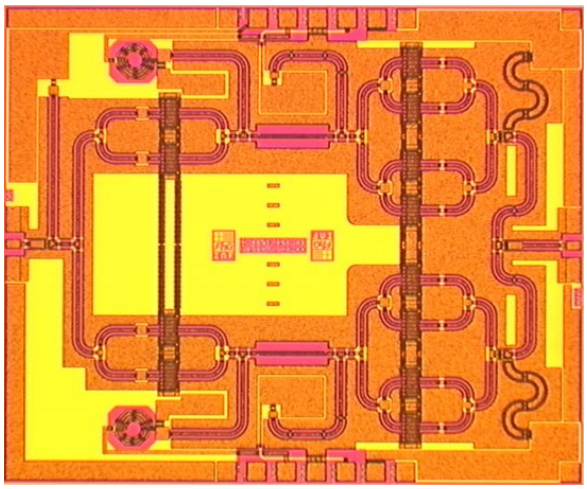

Fig. 8: Photograph of the 1-Watt Ka-band coplanar HPA (the chip size is 2.45 × 2.95 mm²).

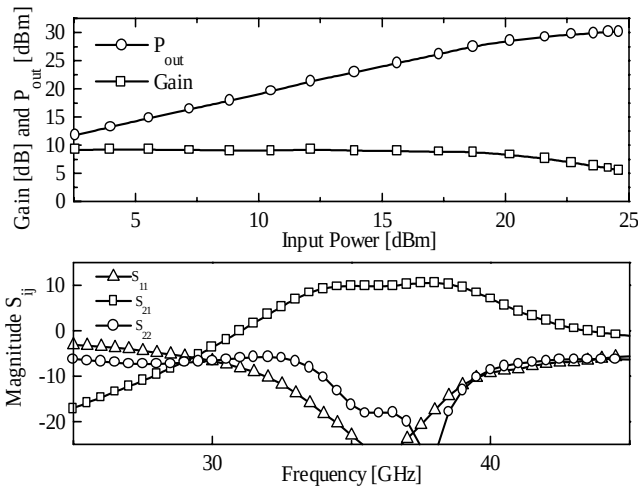

Fig. 9: On-wafer measured output power, linear gain and S parameters of the 1-Watt Ka-band CPW HPA.

IV. CONCLUSION

Active device geometry, mounting conditions and their influence on the temperature profiles and performance of coplanar power devices and circuits have been investigated and verified experimentally, providing a reliable thermal management design database. This resulted in the successful design and characterization of a number of compact coplanar MMIC amplifiers, having high output power in the 20-60 GHz frequency range, and demonstrated the potential of coplanar technology for power applications.

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