Improvements of Thermal Resistance and Thermal Stress in Quasi-Monolithic Integration Technology (QMIT) with a New Fabrication Process

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Abstract: ***Static heat transfer and thermal stress analysis for the new generation quasi-monolithic integration technology (NGQMIT) is presented using a three-dimensional finite element simulator. Effects of different factors and parameters such as the gap between the silicon sidewalls and GaAs-chip (W_g), temperature dependent materials properties, isotropic material properties and backside gold metallization thickness or diamond-filled polyimide are described. It is shown that thermal resistances of 11 °C/W and 8.5 °C/W are possible using 200 µm electroplated gold heat-spreader and diamond-filled polyimide on the backside of the active device, respectively. This promises successful realization of the high frequency circuits containing power active devices using the novel QMIT. In comparison to the earlier fabrication process [1-2], eight times improvement in thermal stress is achieved. This extremely improves lifetime of the packaging. The results of thermal stress simulation are compared with white-light interferometery measurement.***

INTRODUCTION

Influences of temperature and induced thermal stress on electrical and physical performance and reliability of electronic equipment are well known. Emphasis on a deep investigation of these influences in the microwave and millimeterwave applications is much higher than the low frequency applications. In this paper, static heat transfer simulation and induced thermal stress in the NGQMIT have been described.

The earlier concept of QMIT was introduced to overcome the problems of pure MMICs and of the conventional hybrid circuits and use the advantages of both alternatives. Although a few circuits containing low power active devices have been realized, the technology has suffered several shortcomings. Two major shortcomings of the earlier concept were high thermal resistance of the structure and the high induced thermal stress [2].

A novel fabrication process has been introduced for QMIT [3], which not only overcomes these problems, but also minimize the parasitics and enables the realization of the passive elements in this technology for the fist time.

Fabrication process, advantages and more details of the new generation technology have been presented in the reference [3]. Figs. 1 and 2 show a realized microtext-fixture and its cross section view in the coplanar circuit realization of the NGQMIT.

MATERIAL PROPERTIES AND MODELLING CONSIDERATIONS

The QMIT structure is constructed from a silicon substrate (Si-(100)), a GaAs-chip (GaAs-(100)), a spin on polyimide layer and either a plasma enhanced chemical vapour deposition (PECVD) layer of amorphous silicon or an electroplated gold layer.

Semiconductor properties remarkably change with temperature and crystal direction. Considering these facts, properties of the materials involved have been presented in tables I to IV. It is assumed that the silicon substrate and GaAs-Chip exhibit elastic anisotropy and the rest of the materials are isotropic.

In the heat transfer simulation, boundary condition on the surfaces touched with the air is assumed to be natural convection with film coefficient of 10 $W/K.m^2$ and bulk temperature of 300 K. Base plate temperature is 300 K and heat sources have been described in the text.

In the thermal stress simulation, the displacement on some surfaces has been set to zero to fulfill the symmetry in the model and fixation of the model.

STATIC HEAT TRANSFER SIMULATION

In this part, static heat transfer properties of the new generation QMIT structure have been investigated. To compare the thermal properties of the structure

regardless of the transistor gate layout, a thermal resistance is defined. In all the simulation, a 16 fingers Ka-band GaAS-MESFET with power dissipation of 1.4 W and a gate length of 0.25 µm, total gate periphery of 800 µm, height of 100 µm, length of 655 µm and width of 395 µm has been used. Heat source is assumed to be a uniform heat flux on the gate areas. To test the robustness of the transistor model, static thermal simulation for the GaAs-transistor on a perfect heat sink has been performed. Maximum temperature is 447.7 K, which has a good agreement with the data in the manufacturer's data sheet.

Fig. 3 illustrates the maximum temperatures for the new structure of QMIT with Wg of 15 µm as a function of electroplated gold layer thickness. As is shown, a thin layer of gold is adequate for the low and medium power application. The curves implies that most of the thermal resistance results from the layout of gate on the transistor. For a better investigation of the thermal properties of the structure ignoring this effect, a uniform 1 W power dissipation has been applied to the whole surface of the transistor. The resulting maximum temperature difference from the base-plate temperature indicates the thermal resistance of the structure. Fig. 4 shows the thermal resistance of the new generation technology as electroplated gold layer thickness. The structure with a 200 µm thick electroplated gold layer in the backside of the transistor gives a good thermal resistance of 11.2 K/W which mostly related to the thermal resistance of the active device itself.

There are two circuit realization methods in the new structure of QMIT, coplanar and microstrip realizations. Although with a good geometrical design of the coplanar line and polyimide spin on layer, a backside metal can be used without significant effect on the electrical characteristics of the packaging, diamond-filled ployimide can be used to fill the hole in the backside of the transistor. If assume the diamond-filled polyimide mixture has a thermal conductivity of 1000 W/m.K, the structure gives an excellent thermal resistance of less than 8.5 K/W.

THERMAL STRESS SIMULATIONS

For all the thermal stress simulations and measurements, a low noise Ka-band GaAs-pHEMT with gate length of 0.25 µm, height of 100 µm, length of 620 µm and width of 400 µm have been used.

Fig. 5 illustrates the maximum thermal stress curve for the new QMIT structure with 10 µm PECVD amorphous silicon on the backside of the transistor and Wg of 5, 15 and 20 µm. The assumed deposition temperature of amorphous silicon is 60 °C. A higher deposition temperature improves the quality of the deposited silicon and has a minor increase in the thermal stress. The 8 µm thick polyimide layer is gently baked up to 250 °C. The maximum thermal stress is 63.7 MPa, which is eight times smaller than that of the earlier fabrication process of QMIT [2]. This greatly improves lifetime of the packaging.

To measure the displacement, resulting from the thermal stress distribution in the QMIT structure, a white-light interferometery measurement has been used. In this method, two-dimensional mapping of the surface of the silicon wafer at the corner of the transistor has been measured for temperatures between 22 °C to 80 °C. The spin on polyimide is transparent. The displacement measurements are done before spinning of the polyimide layer on the microtest-fixture. The transistor is fixed with a 30 µm thick electroplated gold and Wg of 20 µm. The electroplating was done at 65 °C. Fig. 6 shows the measured and calculated Y component of displacement difference of the point on the corner of the measuring square near to the transistor corner and the point on the middle of the measuring square as a function of temperature. Wg is 20 µm and 30 µm thick plated gold layer is used.

CONCLUSION

Three dimensional finite element static heat transfer and thermal stress simulations for the new generation QMIT have been performed. The measured displacement has been compared with the corresponding calculations. In comparison to the old concept of QMIT, great improvements in thermal resistance and thermal stress have been observed for the new generation. These enable the technology for high power applications and give much better reliability and lifetime of the packaging.

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Table I
Properties of Materials involved

Material	Amorphous-Si	Si-(100)	GaAs-(100)	Polyimide [5]	Gold
Young modulus (Pa)	100e9 [4]	-	-	6.6e9	78e9
Poisson ratio	0.27 [4]	-	-	0.35	0.44
Thermal expansion coefficient (1/K)	Table II	Table II	Table II	3e-6	14.2e-6
Thermal conductivity (W/m.K)	Table II	Table II	Table II	0.14651	320
Elastic constants	-	Table III	Table IV	-	-

Table II
Temperature dependent thermal conductivity and thermal expansion coefficients of silicon and GaAs [6]

Temperature (K)	200	300	400	500	600	700
Silicon thermal conductivity (W/m.K)	188.85	131.26	97.48	75.67	60.65	49.80
GaAS thermal conductivity (W/m.K)	75.44	46.00	32.38	24.67	19.75	16.36
Silicon thermal expansion coefficient (1/K)	1.56e-6	2.63e-6	3.27e-6	3.6e-6	3.86e-6	4.0e-6
GaAs thermal expansion coefficient (1/K)	0.56e-5	0.57e-5	0.59e-5	0.6e-5	0.62e-5	0.63e-5

Table III
Temperature dependent second order elastic constants of Si-(100) [6]

Temperature (K)	200	300	400	500	600	700
C_{11} (Pa)	16.185e10	16.050e10	15.885e10	15.805e10	15.705e10	15.520e10
C_{12} (Pa)	5.880e10	5.825e10	5.800e10	5.695e10	5.615e10	5.600e10
C_{44} (Pa)	8.355e10	8.150e10	7.955e10	7.885e10	7.858e10	7.815e10

Table IV
Temperature dependent second order elastic constants of GaAs-(100) [6]

Temperature (K)	200	300	400	500	600	700
C_{11} (Pa)	11.955e10	11.825e10	11.696e10	11.501e10	11.355e10	11.195e10
C_{12} (Pa)	5.385e10	5.305e10	5.205e10	5.192e10	5.155e10	5.125e10
C_{44} (Pa)	6.015e10	5.925e10	5.865e10	5.759e10	5.625e10	5.569e10

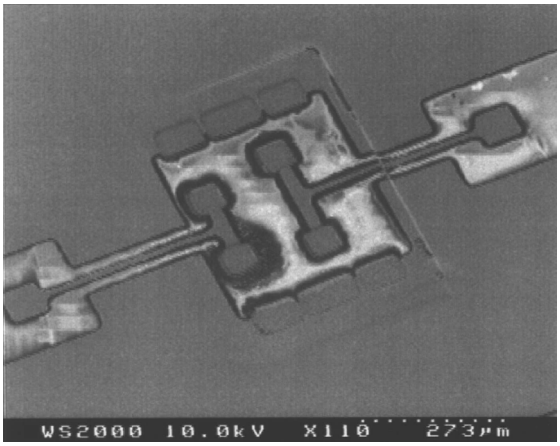

Figure1: *Fabricated microtest-fixture in the coplanar realization of the new generation QMIT.*

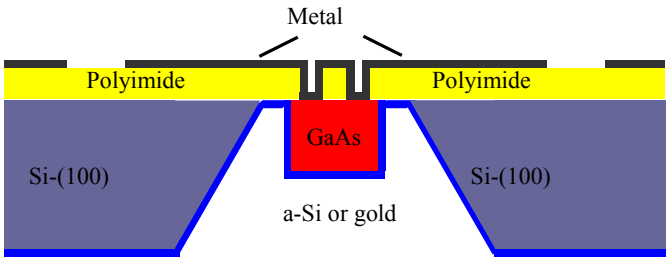

Figure 2: *Cross-section of the microtest-fixture in Fig. 1.*

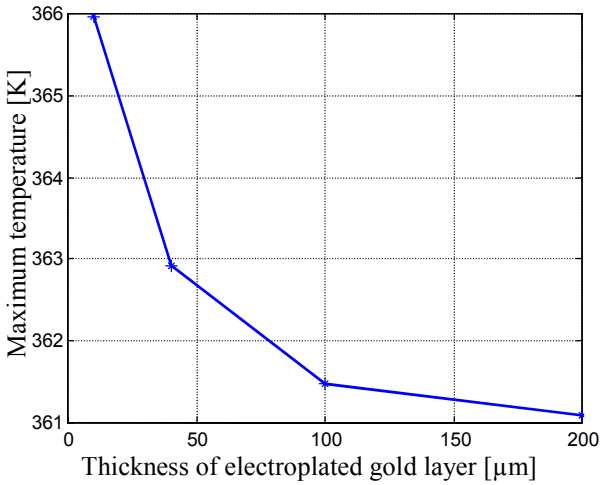

Figure 3: *Maximum temperature in the new generation QMIT as a function of electroplated gold layer thickness. Wg = 20 µm.*

Figure 4: *Thermal resistance of the QMIT structure as a function of electroplated gold layer thickness. Wg = 20 µm.*

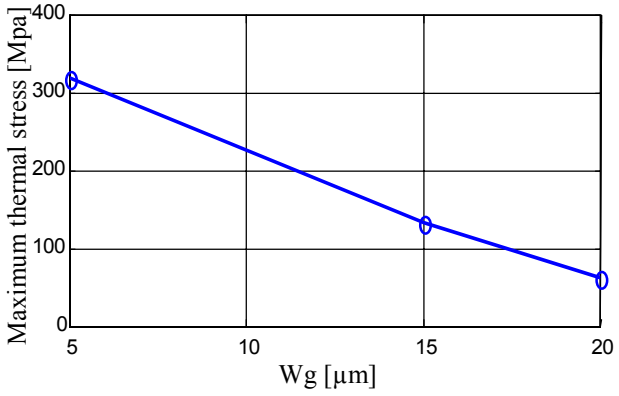

Figure 5: *Maximum thermal stress in the new QMIT for Wg of 5, 15 and 20 µm.*

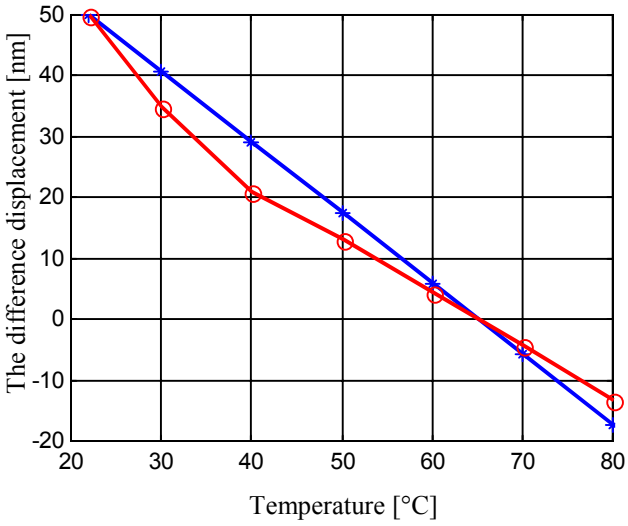

Figure 6: *The difference displacement of the point on the corner of the measuring square near to the transistor corner and the point on the middle of the measuring square as a function of temperature. Wg = 20 µm and 30 µm thick plated gold layer.*