HEMT's Design for Applications beyond 100GHz

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I. Introduction

Electronics up to 100 GHz have applications in atmospheric sensing, radio astronomy, passive imaging applications, wide-band communication systems. Millimeter Wave (MMW) analog and numerical circuits have to be developed. HEMTs on InP substrate are largely used in D-band (110-150 GHz) [1-5] and G-band (140-220GHz) [6-8] circuits. Improvement of frequency operation has been obtained by reduction of gate length to nanometer values [6-7] and higher Indium content up to 80%. Another field of application is induced by the demand of higher bit-rate communication, which is rapidly growing. 40Gbit/s system has been recently developed [9] and intensive research on 80Gbit/s and 160Gbit/s is being done. Analog and numerical circuits used in such optical transmission systems can also be realized with nanometer gate length InP-based HEMTs [10-11]. With InP-based HEMTs, it is possible to reach f_T higher than 472GHz [11] with 30 nanometer gate length. To obtain that good value, gate recess undercut has been optimized.

Cutoff frequency f_T is an important parameter in particularly for numerical circuits. However reduction of gate length will involve an increase of short channel effects. This point will limit the maximum oscillation frequency f_{max} and microwave performance of analog circuits. To avoid this effect, layer structure has to be correctly designed for sub-100 nanometer gate length HEMTs. In this paper, we present an optimized InAlAs/InGaAs/InP layer structure for sub-100 nanometer gate length HEMTs using a scaling down rule. HEMTs have been fabricated on such layer structure and compared with devices fabricated on standard structure usually used for 100 nanometer gate length HEMTs. Same gate lithography of 70 nanometer length has been achieved on both layer structures. DC and microwave characteristics are compared. Degradation of f_{max} in short channel HEMTs can be overcome by the use of transferred-substrate technological process. This technique offers the possibility to realize insulating buffer HEMTs or by the addition of a second gate under the channel, (double gate HEMTs). Technological process and electrical results of TS-HEMTs will be presented in this paper. Finally passive elements and specially transmission lines will be described and presented. These elements are also a limiting factor for the frequency raise of mm-wave circuits. Indeed these passive structures have to present low loss, high characteristic impedance range. Moreover for high speed mixed-mode circuits, these transmission lines have to be blinded to avoid any clock cross-talk phenomena.

II. Design and realization of sub 100nm gate length HEMTs

The increase of the HEMTs performance is possible with obviously the reduction of the gate length, but it's not enough to achieve the best results. The aspect ratio defined as the gate length L_g over the gate-to-channel distance A has to be kept high enough to avoid short channel effects. It is important to find a good trade-off between a high aspect ratio and several physical limitations as the tunneling current across the Schottky barrier, the increase of the quantum energy levels in the quantum well, or the loss of mobility with the reduction of the spacer layer.

On the figure 1.a), we present the standard layer structure currently used for 100 nm gate length HEMTs. In this structure the aspect ratio L_g/A is close to 6 for a 100 nm gate length. For a 50 nm gate length, this value is only 3. To keep a constant value for the 50 nm gate length and so avoid short channel effects, the distance of gate-to-channel A has to be reduced. On figure 1.b), we show the optimized layer structure for 50 nm gate length HEMTs. The gate-to-channel distance can not be further reduced, because of gate tunneling current and depletion from the surface of the carrier in the

channel near the recessed region. To improve Schottky characteristics and the confinement of electrons in the channel, aluminum content in the InAlAs layers has been fixed to a higher value of 0.65. In the channel, we choose an indium content of 0.65 to improve carrier transport properties. Moreover, to avoid degradation due to the depletion of channel induced by the surface states in the recess, we raised the δ-doping at $6x10^{12}cm^{-2}$ for the optimized structure (figure 1.b). To limit parasitic effects, as tunneling current or parasitic conduction in the δ-doping layer, the δ-doping cannot be increased to higher value. Monte-Carlo simulation has been used to confirm choices on this new layer structure. Details and results of simulations are given elsewhere [12].

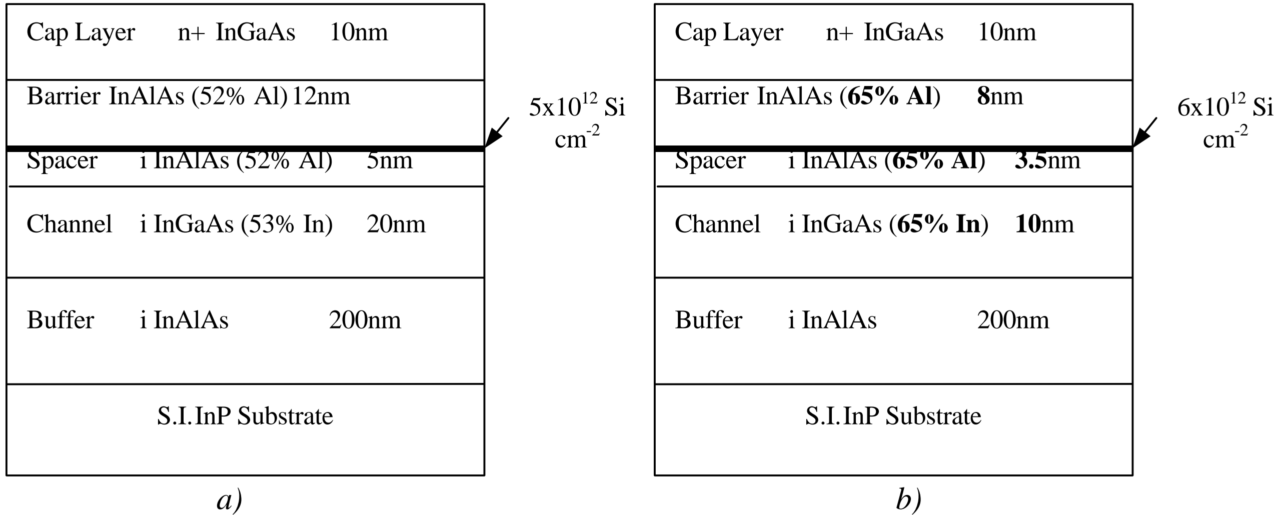

Figure1 : Standard (a) and optimized (b) layer structures.

Standard and optimized structures were realized by molecular beam epitaxy. 70 nm gate length HEMTs with same technological process were fabricated on the standard (figure 1.a) and the optimized (figure 1.b) structures. First the mesa isolation was defined by H_3PO_4:H_2O_2:H_2O solution. Ohmic contact Ni/Ge/Au/Ni/Au was evaporated followed by 1 minute rapid thermal annealing at 310 °C. Typical ohmic contact resistance of 0.15 to 0.2 Ω.mm was measured. The T-shaped gate was defined by electron beamlithography. InGaAs cap layer was selectively removed using succinic acid, ammonia and hydrogen peroxide mixture. Finally Ti/Pt/Au gate was evaporated as well as the bonding pads.

DC characteristics of a 70-nm-gate HEMT on the new layer structure exhibit a maximum transconductance g_m about 1 S/mm. Pinch-off voltage V_p is –0.4 V. Drain-to-source current I_{ds} reaches a value of 560 mA/mm. For the standard structure, V_p is –0.7 V and I_{ds} is 500 mA/mm. The DC-transconductance is about 750 mS/mm.

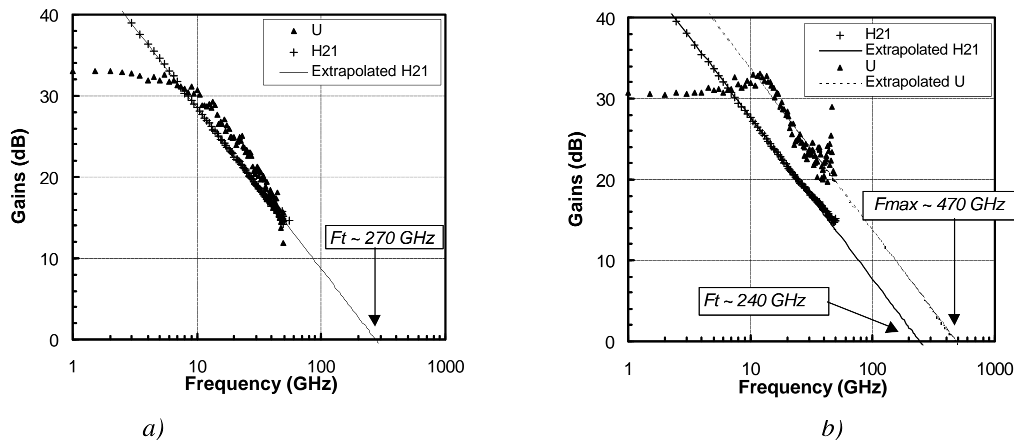

Figure 2 : Performances of 60nm x 100µm HEMT processed on a standard (a) and optimized (b) layer structures .

On-Wafer S-parameters measurements were performed up to 50GHz for both devices. Small signal equivalent circuit has been extracted. On the intrinsic transconductance, a large improvement is

obtained with the optimized structure. Values for the standard HEMTs and the optimized HEMTs are respectively 1180 and 1550 mS/mm. That difference confirms the improvement of the aspect ratio L_g/A of the optimized structure. Figure 2 shows the extrinsic $|H_{21}|^2$ and unilateral gain U versus frequency for the 70nm-HEMTs realized on a standard (a) and optimized (b) layer structure. f_T of the HEMT on the optimized structure is 240GHz. For the standard LM-HEMT, we obtained a f_T of 270 GHz. The maximum oscillation frequency f_{max} for the optimized HEMT is 470 GHz, and exceeds largely the 260 GHz value obtained with the standard structure. This high f_{max} is related to the improved ratios gm/g_d and C_{gs}/C_{gd} (intrinsic values) obtained with the optimized layer (respectively 18.7 and 7.8) in comparison with the standard layer (respectively 6.7 and 5.1). This is due to a reduction of short channel effects and improvement of charge control.

III. Transferred Substrate HEMTs

In sub-0.1 µm gate length device, short-channel effect will be a limiting factor in the improvement of f_{max}. Indeed injection of carriers in the substrate, when shorting gate length, will drastically degrade the output conductance gd of the device The way to suppress injection of these carriers is to replace the substrate by an insulating layer. This can be achieved by a transferred-substrate technique previously used in SOI-MOS and TS-HBT technologies [13].

Lattice-matched InAlAs/InGaAs layers were grown on 2-inch InP substrate by Molecular Beam Epitaxy. In comparison to typical structure used for conventional lattice-matched HEMTs on InP substrate, the heterostructure has been reverse grown. The main difficulty associated with the growth of the reverse heterostructure is the Silicon segregation from the cap layer in the Schottky contact layer and more from the delta-doping plane in the channel layer which drastically reduces the electron mobility. These have been overcome by choosing a suitable growth temperature sequence.

Figure 3 shows the schematic cross section the InAlAs/InGaAs/InP structure transferred on the Silicon substrate. InAlAs/InGaAs/InP HEMTs structure and Silicon wafer were bonded by means of SiO_2-SiO_2 bonding (Thickness ~ 550 nm). 2-inch wafer bonding has been processed at CEA-LETI [14]. Fabrication of HEMTs requires InP substrate and ecth-stop layers removing, to uncover the cap layer. At this step of the process, Hall measurement has been achieved at room temperature, to verify growth quality and influence of bonding. The sheet carrier density and Hall mobility are respectively 3.2 10^{12} /cm^2 and 6900 cm2/Vs. These values are weakly affected by the reverse epitaxial growth, compared with typical values obtained with conventional heterostructure used for LM-HEMTs. Then the 0.12 µm T-shaped gate length HEMT fabrication can be started. It is exactly the same process used on classical LM-HEMTs, reported before.

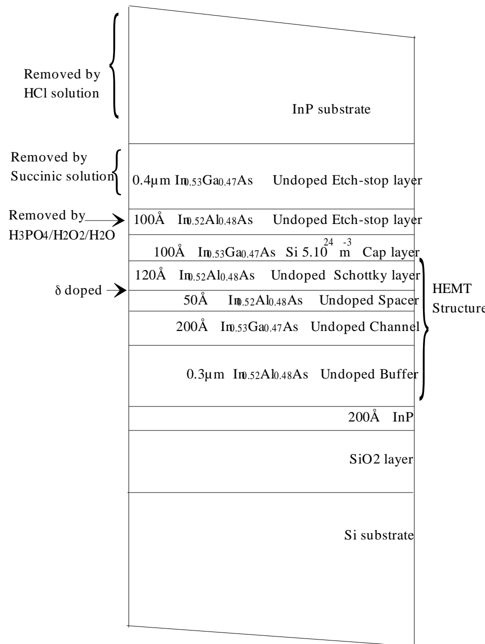

Figure 3 Cross section of HEMTs structure reported on Silicon substrate by SiO2-SiO2 bonding.

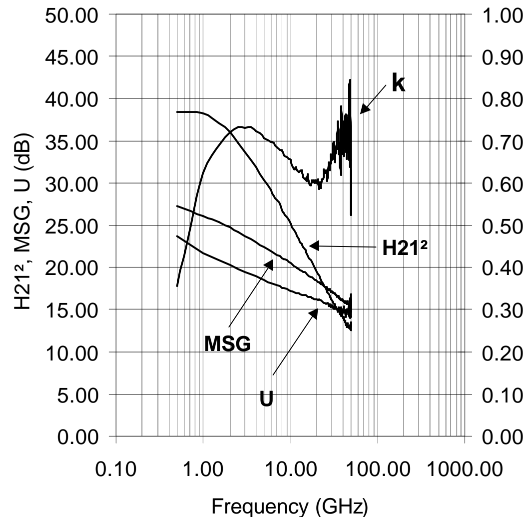

Figure 4 Microwave gains of 0.12µm transferred-substrate HEMTs.

DC and microwave characteristics of 100 µm wide TS-HEMTs were measured on wafer. The device exhibits maximum drain-to-source current I_{ds} = 450 mA/mm. The maximum extrinsic transconductance gm is 770mS/mm. Using S-parameters measurement in the 0-50GHz frequency range, calculated extrinsic current gain $|H_{21}|^2$, maximum stable gain MSG and unilateral gain U are plotted in figure 4 versus frequency. Extrapolation by 20 dB/decade of $|H_{21}|^2$ gives an extrinsic cutoff frequency f_T of 185 GHz. This result is close to published results obtained with LM-HEMT on InP [15]. Maximum oscillation frequency f_{max} deduced from extrapolation by 20 dB/decade of U is 280 GHz. This evidences the growth quality of the reverse heterostructure and shows that the transferred-substrate process affects very weakly the microwave performances of the TS-HEMTs.

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