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C-Band Resistive SiC-MESFET mixer

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Abstract— In this paper the design and characterization of a linear C-band single ended resistive SiC-MESFET mixer is presented. The mixer has a minimum conversion loss of 7.8 dB and has a third order intermodulation intercept point of 30.3 dBm. The mixer is designed using a harmonic-balance simulation load-pull approach. This design method is especially useful for high-level mixers, where small-signal approximations cannot be used.

Index Terms— resistive mixer, silicon carbide, wide band gap semiconductors, intermodulation distortion, high-level mixer, intermodulation intercept point, C-band.

I. Introduction

Silicon Carbide (SiC) devices have foremost found use in high-power applications such as power-amplifiers and limiters. However Fazi [1] made a simple experiment showing that mixers utilizing wide bandgap devices as mixer elements could have better dynamic-range and intermodulation performance compared to mixers using traditional GaAs-technology. This was later demonstrated by Eriksson [2], reporting a single-balanced SiC Schottky diode mixer with a third order intermodulation intercept point (IIP_3) of 31 dBm. Even better linearity can be achieved in mixers using MESFETs operating in the resistive region [3]. We have previously reported a S-band resistive SiC-MESFET mixer with a conversion loss of 10.2 dB and an IIP_3 of 35.7 dBm [4]. This paper extends those results into C-band - while lowering the conversion loss and the LO power requirements. The SiC-MESFET used in this experiment was processed in-house and from the same batch as the transistor used in the previously reported S-band mixer.

Presented is a systematic mixer design method is also presented. This method is suitable for high-level mixers with high power RF excitation and LO drives and could also prove to be useful in designing sub-harmonic mixers etc.

II. Mixer Design

In this section mixer design methods and implementations are discussed.

A. Load-Pull

There are numerous rule-of-thumb guidelines to follow when designing resistive FET-mixers [5]. These rules have been established by performing experimental studies on mixers. Dî Luan used a more systematic approach, although a bit more complicated, involving an active load-pull approach [6]. Optimum load- and source-impedances where found by active- and passive tuning at the transistor terminals. More effective than performing actual load-pull measurements would be to implement this technique into a harmonic-balance simulator. Villemazet used a statistical mixer load-pull method, were the embedding impedances where set by a statistical distribution [7]. A drawback with Villemazets method is that there is no guarantee that the embedding impedance is varied in such a way that the whole Smith-chart is covered.

We have implemented a systematic harmonic-balance based mixer load-pull in commercial Harmonic-Balance simulator. Our method can control embedding impedances at arbitrary many mixing frequencies, is not constrained to any specific device technology (including active) and arbitrary many mixing elements could be used. However as with all simulation-based methods, accuracy is strongly related to the quality of device models used.

First a simulation where the bias is swept is performed - the optimum bias (regarding conversion loss) is then kept for the remaining simulations. Then embedding impedances are processed in the following order (the same as Dî Luan did), while the signal power at the drain terminal is studied at frequencies f_{IF}, f_{LO}, f_{RF}, and f_{2LO}. At each step the embedding impedance that gives the best mixer performance is chosen, where best performance relates to low conversion-loss and low spurious responses. Each impedences take on the initial values tabulated in Table 1.

1. Sweep $Z_{g,LO}$
2. Sweep $Z_{d,RF}$
3. Sweep $Z_{d,IF}$
4. Sweep $Z_{d,LO}$
5. Sweep $Z_{g,rf}$

Optionally sweep Z_{2rf} and Z_{2lo} at both the drain and gate. Our investigation showed that these terminations didn't have any significant impact on mixer performance. In Figure 1 and 2 typical outputs from step 3 and 4 are displayed. Notice how the well-known results, that the IF should be terminated at high-impedance for low conversion-loss and

TABLE I
LIST OF FREQUENCIES AND DEFAULT EMBEDDING IMPEDENCES

	Frequency [MHz]	Mix-Index		Z_G [Ω]	Z_D [Ω]
f_{IF}	300	-1	1	50	50
f_{2IF}	600	-2	2	50	50
f_{LO}	5000	1	0	50	short
f_{RF}	5300	0	1	short	50
f_{2LO}	10000	2	0	50	50
f_{2RF}	10600	0	2	50	50

that the drain should have a short-circuit at LO for low power at the second LO-harmonic, are described by this method.

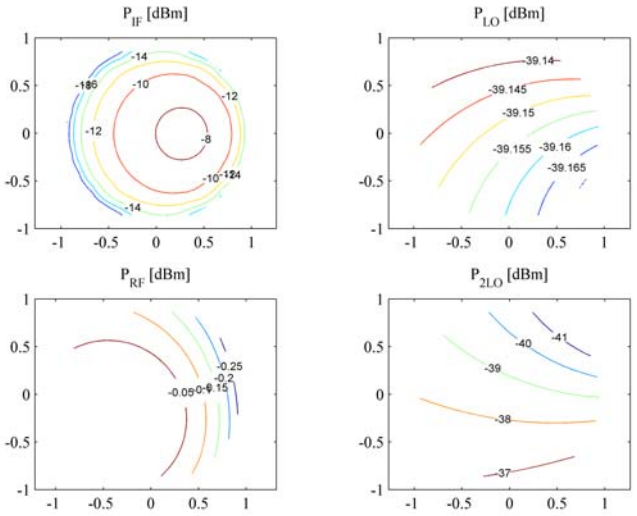

Figure 1. Example of power contours in $\Gamma_{D,IF}$-plane. Notice the well-known optimum for high-impedance IF-load (top left).

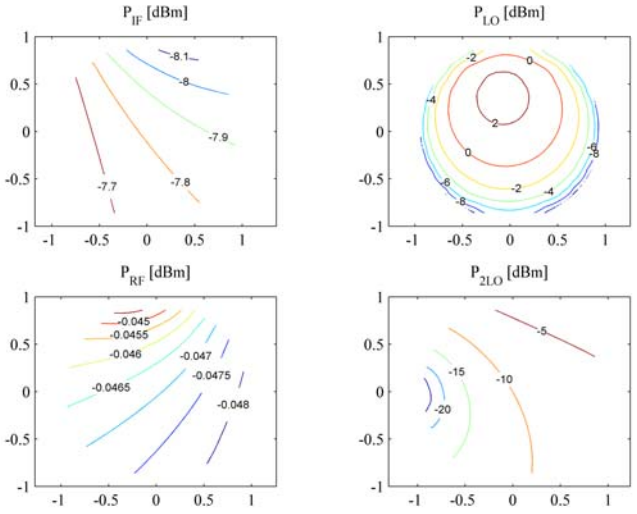

Figure 2. Example of power contours in $\Gamma_{D,LO}$-plane. Notice the well-known optimum for short-circuiting the drain at LO (bottom right).

B. Implementation

The designed mixer is implemented as a hybrid circuit on a soft substrate (IsoClad933, εr=2.33). Gate termination at f_{LO} and f_{RF} are realized by a periodic open-stub configuration using three stubs. Drain termination are realized at f_{LO} and f_{RF} with a folded two section coupled Chebysheff band-pass filter and two additional open-stubs. The f_{IF} termination is done by a quarter-wave length (at approx. f_{RF}) high impedance line and with two open radial-stubs for terminating f_{LO} and f_{2LO}. Gate bias is fed through two 5k-ohm resistors and a high impedance quarter-wave section with an open radial-stub, additional capacitors are used for decoupling. As DC-block at the LO-port a 6.9 pF capacitor is used.

The substrate is soldered to a gold-plated brass plate. The SiC-MESFET are glued to a ridge on the brass plate and wire-bonded into the circuit. Through-plated via-holes are used for ground connections thru the substrate.

III. MIXER CHARACTERIZATION

The mixer was biased at –6.5 V and the conversion loss versus RF-frequency (for fixed IF-frequency) was measured. As can be seen from Figure 3, minimum conversion loss is obtained at f_{RF}=5175 MHz and f_{IF}=250 MHz rather than at f_{RF}=5300 MHz and f_{IF}=300 MHz as designed. This is most probably caused by a shift in the pass-band characteristics of the RF band-pass filter.

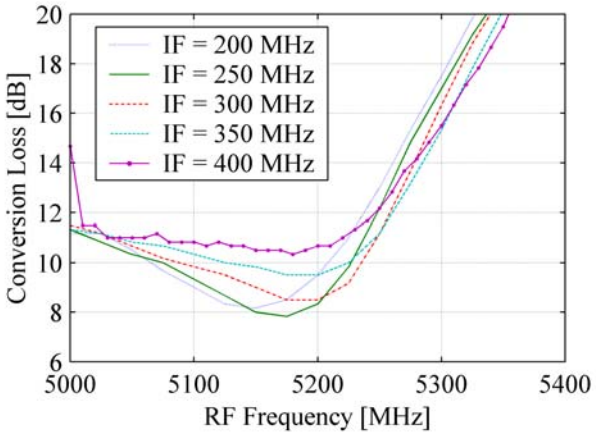

Figure 3. Conversion Loss versus RF-frequency (for fixed IF-frequency), V_{gs}=-6.5 V, P_{LO}=23 dBm and P_{RF}=0 dBm.

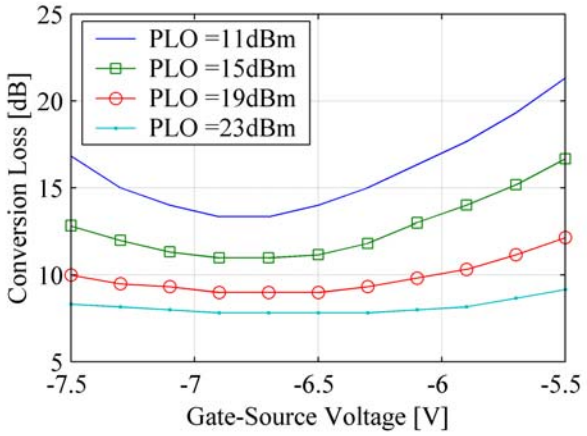

Figure 4. Conversion Loss versus Gate-Source Voltage, P_{RF}=0 dBm, f_{RF}=5175 MHz, f_{LO}=4925 MHz.

With the optimum frequencies, conversion loss (CL) versus gate-source voltage is measured. This measurement is repeated for different LO power levels, c.f. Figure 4. Minimum conversion loss is 7.8 dB at V_{gs}=-6.5 V with an LO power of 23 dBm.

For optimum bias, CL measurements versus LO and RF power is made (Figure 5). For high LO drive (e.g. >18 dBm) CL is practically independent of RF power.

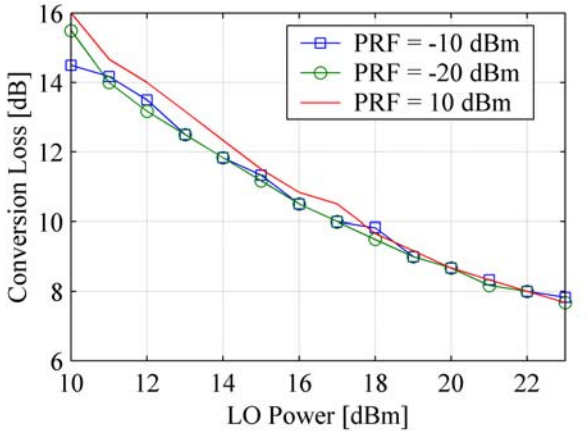

Figure 5. Conversion Loss versus LO power, V_{gs}=-6.5 V, f_{RF}=5175 MHz and f_{LO}=4925 MHz.

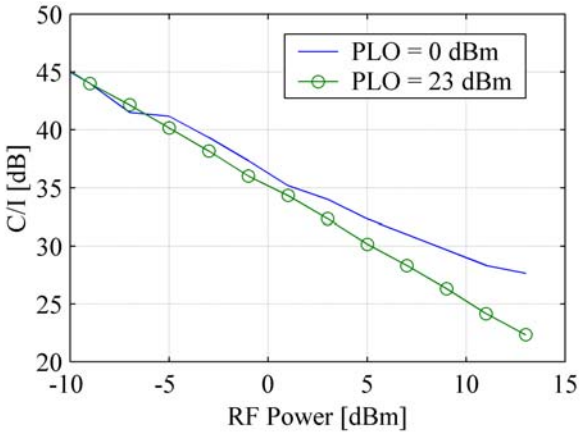

Figure 6. Carrier to Intermodulation ratio versus RF power, V_{gs}=-6.5 V, f_{RF}=5175 MHz and f_{LO}=4925 MHz.

Second order intermodulation is measured; in Figure 6 the carrier to intermodulation ration (C/I) is plotted versus RF power – giving a second order intermodulation intercept point of 34.8 dBm.

Third order intermodulation products are measured using a two-tone test. The two equal power RF-signals are separated by 10 MHz (f_{RF1}=5175 MHz, f_{RF2}=5185 MHz). Carrier to intermodulation ratio is measured for two different bias voltages: -6.5 V and –7.7 V (Figure 7 and Figure 8). The latter resulted in significant reduction of unwanted sidebands, especially for low LO drive and high RF power, e.g. at mixer compression. This is most probably due to reduced rectifying of the LO at the gate. At bias equal –6.5 V the maximum extrapolated third order intermodulation point was 30.3 dBm. The 1 dB IF-compression point for two carriers is 16 dBm, giving an estimated single carrier compression point of roughly 19 dBm.

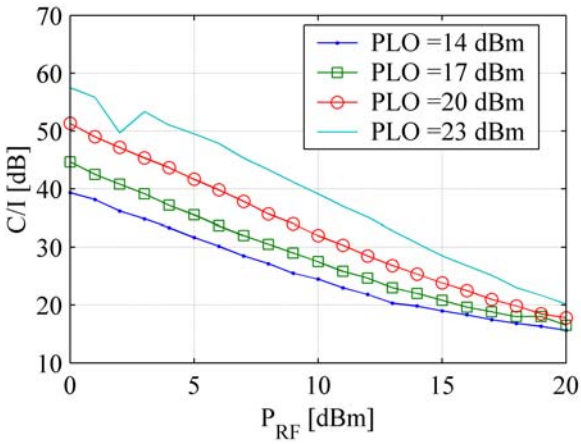

Figure 7. Carrier to Intermodulation ratio versus RF power, V_{gs}=-6.5 V and f_{LO}=4925 MHz.

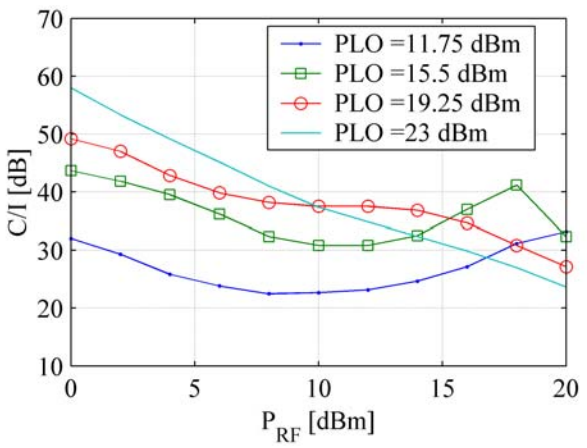

Figure 8. Carrier to Intermodulation ratio versus RF power, V_{gs}=-7.7 V f_{LO}=4925 MHz.

IV. Conclusions

The design and characterisation of a linear C-band resisitve SiC-MESFET mixer were presented. The mixer had a minimum conversion loss of 7.8 dB (including losses at input and output), the maximum third order intermodulation intercept point was 30.3 dBm and the estimated 1 dB compression point is 19 dBm.

This is to our knowledge the first mixer reported using SiC-based mixing elements above 4 Ghz. It is also believed that IIP3 as well as CL of this mixer could be improved by even higher LO drives than 23 dBm, indicated in Figure 5, where CL is not in full compression as were the case in the S-band mixer.

The proposed mixer load-pull method has to be further investigated; primarily since the RF band-pass filter didn't fulfill the design specifications and therefore not had the correct embedding impedances.

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