Fast Tuning Electronically Switched 16 x 1 Channel Receiver For Packet-Switched WDM Systems

S. K. Manfrin*, M. De Dominicis, G. Orengo, F. Giannini, M. A. Romero**

Department of Electronic Engineering, University of Rome "Tor Vergata", Via Politecnico 1, 00133, Rome, Italy, tel. +39 06 7259 7345, fax.7343, e-mail: orengo@ing.uniroma2.it

* Centro de Pesquisa e Desenvolvimento de Informática e Automação - CPDIA, Praça das Orquídeas, 44/52, CEP 06453-000, Alphaville, Barueri, SP, Brazil, email: smanfrin@sel.eesc.sc.usp.br

** Department of Electrical Engineering, University of São Paulo, Av. Dr. Carlos Botelho, 1465, CEP 13560-970, São Carlos, SP, Brazil, e-mail: muriloa@sel.eesc.sc.usp.br

This paper revisits an optical receiver topology, for a wavelength division multiplexing (WDM) optical network at 2.5 Gbps bit rate, based on non-tunable wavelength demultiplexing and electronic switching. We demonstrate novel, monolithically integrated, four-channel optical receiver module composed of MESFET transimpedance amplifiers and switches that can be independently switched "on" or "off" electronically by a digital signal. The selector chips have also been reconfigured as a 16 channel selector array. Frequency and noise performance as well as switching speed and crosstalk between neighboring channels have been investigated.

INTRODUCTION

WDM networks require compact, low-cost wavelength selectors or tunable filters capable of covering a wide spectral range with a narrow bandwidth. Also, in a packet-switched environment, the channel reconfiguration time must be a fraction of the packet length, in order to assure a reasonable throughput. Further requirements of the tunable receiver include a large number of channels, polarization insensitivity, compactness, low loss, low crosstalk, low power consumption and low manufacturing cost. These requirements render various existing tunable filters inadequate for such networks.

With the goal of overcoming these difficulties, an alternative approach to tunable optical filters for the task of optical channel selection has been demonstrated to be an electronic front-end receiver which can be combined with an optical demultiplexer to select incoming wavelength channels by electronically switching of the detector array (1,2). The resolved optical channels are coupled to photodetectors and connected to a front-end amplifier via integrated electronic switches. Only one switch is activated at a given time so that only one photodetected signal can be amplified and the electronic channel selection can be performed in the range of a few nanoseconds.

A further consideration regards the number of input switches, that is equal to the number of input wavelength-division optical channels. Each additional MESFET switch, in fact, increases the capacitive loading to the selector/receiver and causes a degradation in system performance. However, electronic front-end selectors should be able to resolve a large number of input WDM channels. To this aim, in this paper we assembled and tested a hybrid configuration (3) composed of cascaded 4x1 monolithic integrated front-ends to perform 16x1 channel selection. Frequency and noise performance as well as switching speed and crosstalk between adjacent channels have been investigated.

ELECTRONIC FRONT-END SELECTOR

Figure 1 shows a proposed circuit schematic of the electronic selector chip proposed in reference (2). Each one of the FET switch can be connected from the input side to the corresponding off-chip photodetector that can receive an individual wavelength channel. In order to avoid the high insertion loss observed in the above configuration a distinct 4x1 channel selector topology has been previously implemented by us (1). The circuit schematic is shown in Figure 2.

In the first circuit proposed four input MESFET switches share the same transimpedance amplifier. However, this configuration suffers from a high insertion loss due to its "passive" switching circuitry, which, in our case, it consists of three FETs of 300 μm gate width connected in series-shunt-series fashion. In the second case, Figure 2, each electronic channel has its own transimpedance preamplifier and FET switching circuit. The two receiver configurations have been demonstrated to achieve similar RF and switching performance (1) but different noise levels are expected. Input switches are, in fact, seen in series from the input noise current in the first circuit. Thus, they do not add to amplifier and photodiode noise current at low frequency. However, as the frequency increases, the shunt effect of parasitic capacitances increase its

noise contribution. For this reason, we expect the second topology to be more efficient in terms of receiver sensitivity, despite higher power consumption and chip area as it will be seen in the next section. Therefore it can be an adequate solution for those applications in which sensitivity is of primary interest. The design aims at operation at 2.5 Gbps.

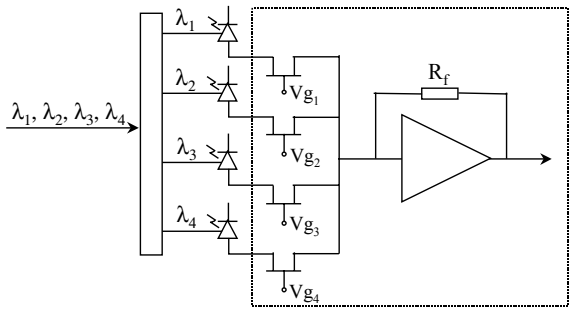

Figure 1: First front-end configuration for a 4-channel electronic selector (FE1).

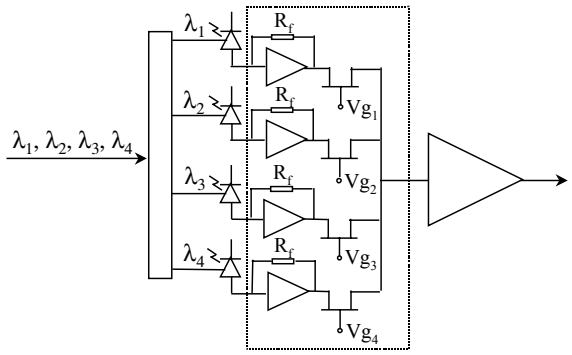

Figure 2: Second front-end configuration for a 4-channel electronic selector (FE2)

Next, a composite hybrid architecture implementing a 4x4x1 electronic selector has been realized cascading two switch stages. The schematic diagram is shown in Figure 3. The first stage switches select four channels among 16 input channels, the same channel in each 4x1 selector chip, which shares a common control. The second stage selects the input chip selector. Altogether, five chip selectors and eight control voltages have been used.

EXPERIMENTAL RESULTS

For testing purposes, each one of the two four channel MMIC front-ends was wire bonded on a two-channel test fixture. Two power supplies (V_g and V_{dd}) plus six high speed SMA connectors (two for I/O signals and four for the switch controls) were connected to the fixture. The bias voltages of the receiver were chosen as V_{dd} = 6 V, V_g = -1 V.
Preliminary results comprising the microwave circuit performance and the switching capability for an 1 Gbps input signal have already been previously reported (1). The receiver showed a uniform 3-dB frequency response of 2.5 GHz. The transimpedance gain was 50 dBΩ. The output power level of the isolated channels were at least 60 dB below the power level for the connected channels.
Here, the input equivalent noise current density has been measured on both chips and the results are shown in Figure 4. The second receiver configuration has demonstrated to reduce the average noise at high frequencies at the expense of power consumption, increased circuit complexity and chip area which goes from 2.27 mm^2 up to about 4.49 mm^2. It is believed that this trade-off can be satisfactory in high-performance applications.

The performance of the 16x1 channel selector realized with two switch stages has been also investigated. The overall 3-dB bandwidth and transimpedance gain has been measured to be in excess of 2 GHz and 60 dBΩ, respectively. The output response to input switching packets is shown in Figure 5. The switching speed both at the first and second stage switches has been measured for an input sinusoidal signal at 2.5 GHz and -5dBm electrical power, by driving control signals with a pulse generator. Using 1-ns rise and fall time, the channel reconfiguration times are found to be around 2 ns for both stages. The switching speed of the channel selection can be faster than 1 ns, and it is mainly limited in this case by the supplied switching power. This switching speed capability is an attractive feature for optical interconnections in supercomputer systems as well as ATM-PON applications (4),(5).

Finally, in order to investigate the electrical crosstalk between neighboring channels connected to the same amplifier we measured the response of one channel at a frequency of 2.5 GHz while a second asynchronous input signal of 0 dBm at 1 GHz is incident on an adjacent switched-off channel. The first channel was biased alternately between the “off” and “on” states through the control switch. There is no distinguishable degradation in the output response observed compared to the results with just one optical input. That is, the sensitivity penalty from the adjacent switched-off channel is below 0.1 dB.

CONCLUSIONS

In conclusion, we have demonstrated two configurations for a monolithically integrated and electronically switched four-detector receiver array, which is capable of random access selection of a single channel for fast packet-switched WDM networking applications. This receiver has a -3 dB bandwidth of 2.5 GHz with a transimpedance gain of 50 dBΩ. The switching speed of the channel selection in this multichannel receiver is, in general, faster than 1 nS. We have also characterized a 16-channel GaAs amplifier/selector chip obtained with an hybrid configuration of cascaded four-channel chips. This could provide low-cost reliable tunable receivers for optical 4-to-16 channel selection and detection.

ACKNOWLEDGEMENTS

This work was supported by FAPESP (São Paulo State Research Foundation) and University of Roma Tor Vergata. The authors would like to acknowledge Prof. M.Cirillo for the mask processing, the Mechanical Lab. of the University of Roma 2 for the test fixture fabrication, and the R&D Center of AMS (Alenia-Marconi Systems) of Rome for the careful test fixture assembly.

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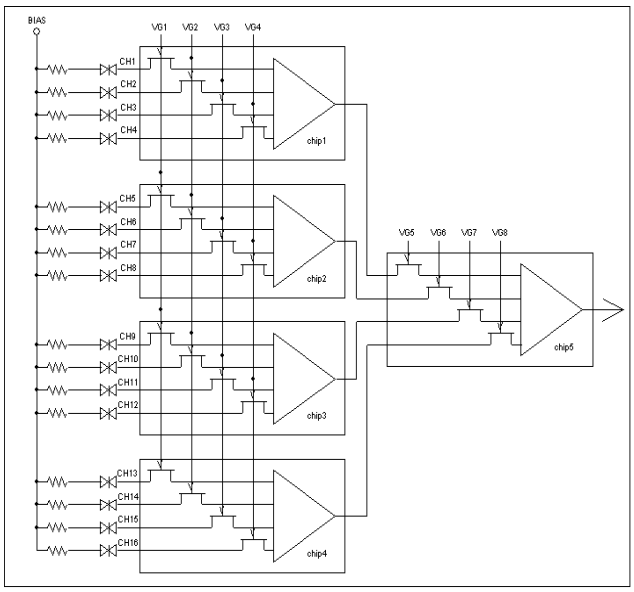

Figure 3: Front-end architecture for a 16-channel electronic selector.

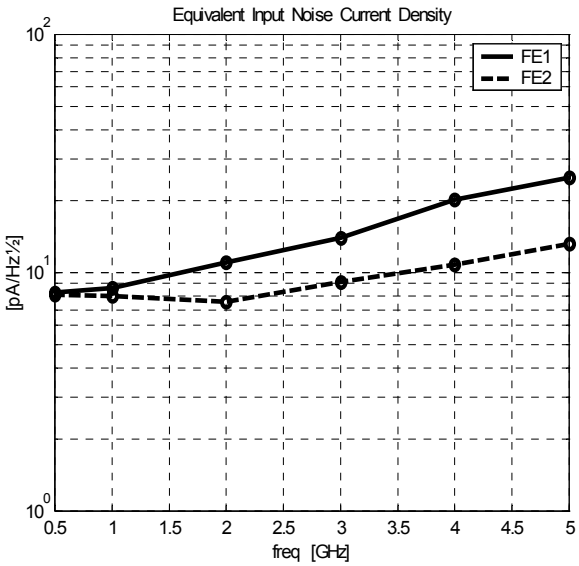

Figure 4: Equivalent noise current measurements for FE1 and FE2 chip selectors.

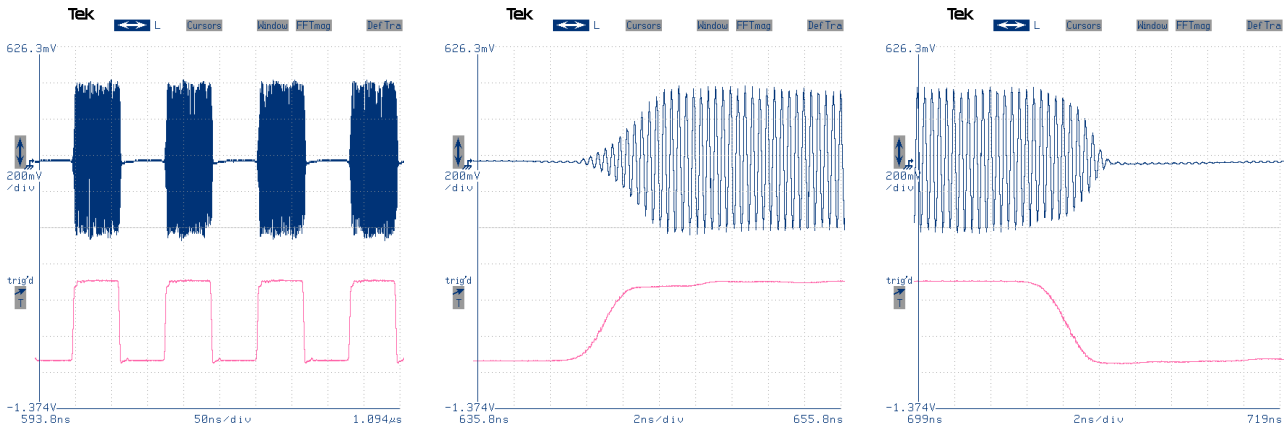

Figure 5:Output response of the 16-channel selector to input switched packets at 2.5 GHz.