A Technique to Design MMICs for Space Applications and High Production Yields

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Abstract

In this paper a MMIC design technique, oriented to the optimization of the production yields, is illustrated together with the obtained results.
This method, based on a sensitivity analysis, i.e. on the circuit behavior for variations of passive elements from their nominal value, and on the contemporary determination of the production yields, allows the identification the circuit elements to obtain high production yield. Moreover it allows an appropriate choice of the circuit topology.
As example, this technique has been applied to design a MMIC to be employed on equipments where a high number of devices is required.

1. Introduction

In the last years the number of required services (tv transmissions, phone communications, multimedia etc.) has grown as well as the number of required equipment per satellite. As a consequence, in alignement with the evolution of the technologies MMIC size reduction in particular at component level is required.
The new challenge is then: to keep a low cost and reliability increasing at the same time the production rate.
The strategy in pursuing this goal could lie not only in using a totally automatic approach in production, but also in performing accurate forecast already at design stage. The first avoids whichever type of operation once that the equipment has been mounted, while the latter allows a yield optimization through an accurate forecast of all the causes of spread and malfunctioning at simulation level.
The yield optimization becomes evident considering the small quantity of MMIC required for space applications compared with those for commercial applications. Since the wafer cost is a fixed parameter, to optimize the yield with the minimum production it is necessary to reduce the circuit sensitivity with respect to the process variations.
This paper presents a MMIC whose design technique has been oriented as mentioned in order to optimize the production yields on a limited number of wafers.
The method is based on a sensitivity analysis checking the circuit behavior including all the variations of passive elements from their nominal value. This allows at the same time the determination of the production yields and the identification the circuit elements to increase it as more as possible. Moreover it allows the choice of the best appropriate topology relevant to the particular application.
The mentioned MMIC was designed for relatively high volume space production as TR Module for a Synthetic Aperture Radar (SAR).

2. Production yield analysis

Using the current simulation tools and starting from the experience and technological data, it is possible to simulate the different working conditions of a MMIC when the technological parameters vary and thus, optimize the design for high yield. To better understand how the mentioned technique can be effectively used, let's give the definition of yield.
The production yield can generally be classified into four categories [1]:
Fabrication Yield: i.e. yield of the whole wafer during the fabrication process
Component Yield: i.e. yield of the single circuit inside the wafer, limited by the defects of the MMIC's components (FET, capacitors, inductors, resistors), which has a partially or totally incorrect DC and RF working condition as a result.
Specification Yield: i.e. yield of the single circuit inside the wafer working in DC and RF outside the specifications imposed during the design; this yield is influenced by the fabrication tolerances of the single devices.
Other Yield Loss: i.e. yield determined by other causes like, for example, physical defects of a working device, not acceptable from a quality point of view.

Some remarks is necessary to understand where and how to act in order to improve each of the foregoing yields.
The Fabrication Yield tends towards a natural improvement as much as the fabrication process becomes mature. A similar behavior can also be observed for the Other Yield Loss and, in a less amount, for the Component Yield.
On the contrary, the Specification Yield is the only one that can be controlled and so the design technique we propose aims to control and improvement of this yield.

3. The design approach

Generally speaking, the approach used to design the MMIC can be summarized as follows:

1. Analysis of the lumped parameter circuit

This preliminary phase allows to establish the range of performance and select the most suitable circuit topology for the matching network to meet the required specifications

2. Analysis of the distributed parameter circuit

In this case the passive components (capacitors, inductors, resistors), which were considered as ideal elements during the previous phase, are substituted by real elements with models developed by the foundry. This analysis allows to understand which topology is the less sensitive to the process variations and so, matching the requirement of high production yield.

3. Layout design

The actual placement of the layout allows to know the parasitic effects due to the connections. Presently available software allows to continuously link and simulate schematic and relevant layout at the same time. With the inclusion of all the parasitic elements, the circuit behavior will be different from the one estimated during the design and it will be necessary to modify the single component sizes, until the project specifications are meet.

4. Sensitivity analysis

Once the the circuit is finished (electrical and layout phase), the sensitivity analysis is performed. In this case the behavior of the circuit corresponding to the passive component variations from the nominal values can be verified. At the same time, the production yield can be calculated, checking that the results are satisfactory. If not, it is necessary to act on the detected sensitive points of the circuit to improve the yield.

4. Numerical simulations and results

Initial electrical requirements for the designed MMIC are reported in Tab. I.
The chosen process was a well assessed Low Noise PHEMT having the following caracteristics: Gate length = 0.25 um, Noise figure = 2dB @ 40 GHz , Associated Gain = 10 dB, 330 pF/mm , Power density = 0.30 mW/mm, max usable Frequency = 60 GHz.
A two stage approach was necessary to obtain the required performances. The two active elements are made of two multifinger MESFETs having gate 4x 25 μm and 4x75 μm respectively. High value resistors were used for the gate biasing. High precision Tantalum nitrate have been used for source biasing. The schematic of the circuit is reported in Fig. 1.

4.a Sensitivity analysis

It has already been pointed out that the Specification Yield is the yield on which the proposed design technique is applied. It should also be noted that the foundry guarantees the active and passive realization according to the specified sizes within given tolerances. In fact, the Spread Parameters are included in the data referred to those elements, representing the spread of the single component value around the design nominal value. Thus, it is supposed that the value of the single device is characterized by a distribution of probability, which is gaussian, having mean equal to the component nominal value, and standard deviation σ equal to the spread parameter.
Furthermore, for each spread parameter an on-wafer and a wafer-to-wafer value is extracted. This distinction is due to the fact that during the device fabrication, there is a variation also among different wafers. Only for the inductors the same values are given in both cases, one referred to the inductance (DL) the other to the equivalent resistance (DR) associated to the component.
The data provided by the foundry are given in Tab. II.
Once the values have been set for each single component, a statistical simulation can be performed using a standard simulator. We used LIBRA® Series IV compiled with smart library provided by the foundry. A given number of random samples are generated and, for each component, the simulator selects a value within the gaussian distribution range.
The circuit behavior can be analyzed to verify the sensibility with respect to those variations. At the same time the production yield is evaluated defining the range within which the specification must be included in order to consider the chip acceptable for the specific application. Histograms can be generated for each parameter as S_{21} ,S_{11} and S_{22}
Nevertheless, it should be noted that, due to the limitation of the simulator, the analysis of the S_{21} in terms of ripple was performed using a different approach. The standard simulator we used permits only to check if the amplifier gain is

contained within two given values, A and B, where B is greater than A, but it is not possible to perform the yield on a parameter linked to an equation. This, in turns, could generate mistakes in the final MMIC selection.
To overcome this problem, a program has been realized using MATLAB® to calculate the yield with reference to the specification on the gain and on the ripple of the amplifier, and to elaborate the data produced by the statistical simulations performed by LIBRA®.
The realized program calculates the maximum and minimum value of the gain S_{21}, assuming the minimum as the amplifier gain. In this way the ripple is also evaluated as difference between the maximum and minimum value of S_{21}.
In order to accept the circuit it is necessary that the gain is greater than the design specification and the ripple less the given specification (see Tab. I).
Concerning the production yield calculation, two sensitivity analysis have been performed, one on-wafer, the other wafer-to-wafer and from them $R_{tot,on}$ and R_{tot,w_to_w} have respectively been extracted. Each value represents the total yield under the two conditions.
Those yields are the results of five factors:
R_{S11}: yield referred to the input loss;
R_{S22}: yield referred to the output loss;
R_{S21}: yield referred to the gain;
R_K e R_{B1}: yield referred to the unconditioned stability [2].
Thus:

$$R_{TOT,on} = R_{S11,on} \cdot R_{S22,on} \cdot R_{S21,on} \cdot R_{K,on} \cdot R_{B1,on}$$

and similarly

$$R_{TOT,w_to_w} = R_{S11,w_to_w} \cdot R_{S22,w_to_w} \cdot R_{S21,w_to_w} \cdot R_{K,w_to_w} \cdot R_{B1,w_to_w}$$

The overall yield is given by:

$$R_{TOT} = a \cdot R_{TOT,on} + b \cdot R_{TOT,w_to_W} \quad (1)$$

i.e. it is a weighted mean of the total on-wafer and wafer-to-wafer yield, where a and b have been fixed at 0.5.
The first case taken into account refers to the sensitivity of the circuit designed considering the tolerances only of the passive components, reported in Tab. II. The tolerance on the width W of the MESFET's fingers is not accounted for in this phase. The results that have been obtained are shown in Tab. III
The total yield equals 69.85% according to (1).
The final results on the production yield calculated in the mentioned conditions are summarized in Tab. IV.
Fig. 2 shows the realized MMIC photo. As mentioned, the MMIC size has been increased to keep the alignment with other MMIC present on the same reticle. Optimized matching networks are very compact and it can be seen from the photo the actual chip area can be reduced up to the 50%. This means that the overall MMIC cost can be strongly reduced keeping the same performances. According to the measurements, total obtained yield is 60%. Measured average gain and return losses are reported in Figs.3 and 4 and are quite in accordance with our simulations.

5. Conclusions

In this paper a technique has been presented for high yield MMICs design. It is based on the optimization of the production yield, particularly of the Specification Yield, which is affected by the tolerances of the fabrication of the single components. In the design of MMICs for satellite devices, this results very important as well as the introduction of other parameters such as reproducibility and reliability which concur to the determination of the final production yield.
The proposed technique is based on the statistical sensitivity analysis, i.e. the verification of the circuit behavior as a consequence of the variation of the values of the passive components from their nominal value, and at the same time on the calculation of the production yield. Recently developed software tools allow to apply this technique very easily.
Through this iterative method it is possible to detect the most sensitive points of the circuit, and chose of the most suitable circuit topology to increase the total production yield. Good results have been obtained in a multiproject production also with small quantities showing the usefulness of the method.

References

[1] Wang Y., Zhu L. High Yield MMIC Design Using Improved Random Walk Approach. *Proceedings of Asia-Pacific Microwave Conference*, Adelaide, 1992.
[2] Gonzales G. *Microwave Transistor Amplifiers Analysis and Design*. Prentice Hall, Second Edition, 1997.

Operating Bandwidth	**8 –12 GHz**
Gain S_{21}	**16 dB**
Gain Ripple	**0.5 dB/pp**
Input matching value S_{11}	**<-12 dB**
Output matching value S_{22}	**<-15 dB**
Positive Biasing Voltage	**5 Volts**
Current consumtion	**< 100 mA**

Tab. I - Specifications of the amplifier.

Components	**σ on-wafer**	**σ wafer-to-wafer**
Inductance	**DL=5% DR=20%**	
Capacitor	**2%**	**5.6%**
Resistor in TaN	**2%**	**3.6%**
Resistor in TiWSi	**6%**	**8%**

Tab.II. - Spread parameters by the foundry.

on_wafer	**Pass**	**Fail**	**Yield**	**w_to_w**	**Pass**	**Fail**	**Yield**
$R_{S11,on}$	200	0	**100%**	$R_{S11,w\ to\ w}$	199	1	**99.5%**
$R_{S22,on}$	200	0	**100%**	$R_{S22,w\ to\ w}$	194	6	**97%**
$R_{S21,on}$	151	49	**75.5%**	$R_{S21,w\ to\ w}$	133	67	**66.5%**
$R_{K,on}$	200	0	**100%**	$R_{K,w\ to\ w}$	200	0	**100%**
$R_{B1,on}$	200	0	**100%**	$R_{B1,w\ to\ w}$	200	0	**100%**
$R_{TOT,on}$	-	-	**75.5%**	$R_{TOT,w\ to\ w}$	-	-	**64.2%**

Tab. III - Production yields.

on_wafer	**Pass**	**Fail**	**Yield**	**w_to_w**	**Pass**	**Fail**	**Yield**
$R_{S11,on}$	199	1	**99.5%**	$R_{S11,w\ to\ w}$	200	0	**100%**
$R_{S22,on}$	194	6	**97%**	$R_{S22,w\ to\ w}$	185	15	**92.5%**
$R_{S21,on}$	136	64	**68%**	$R_{S21,w\ to\ w}$	112	88	**56%**
$R_{K,on}$	200	0	**100%**	$R_{K,w\ to\ w}$	200	0	**100%**
$R_{B1,on}$	200	0	**100%**	$R_{B1,w\ to\ w}$	200	0	**100%**
$R_{TOT,on}$	-	-	**65.7%**	$R_{TOT,w\ to\ w}$	-	-	**52%**

Tab. IV - Production yields accounting for the active components.

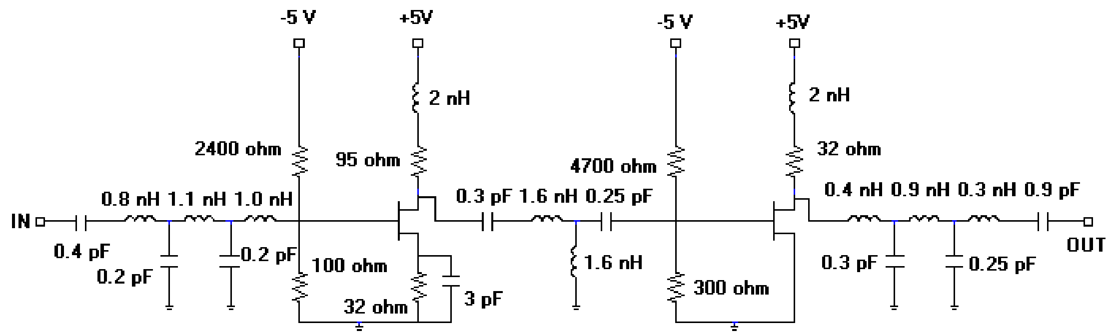

Fig. 1 – Amplifier circuit.

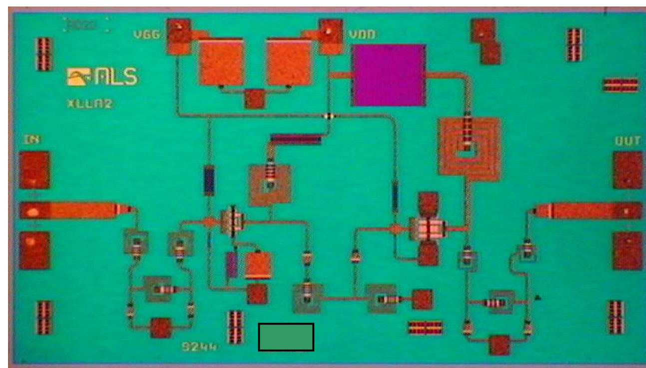

Fig. 2 – Realized amplifier chip.

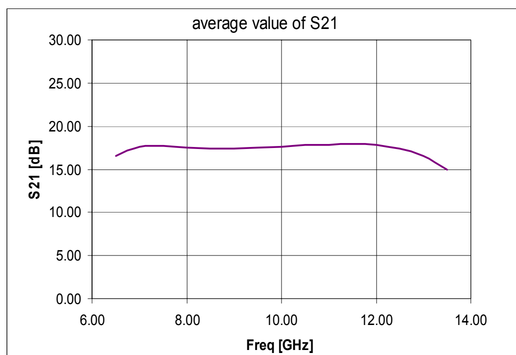

Fig. 3 – Measured average gain of the realized amplifier.

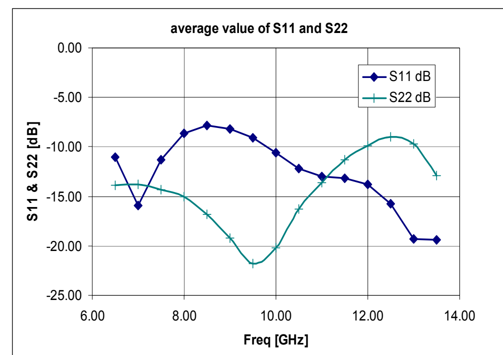

Fig. 4 – Measured return losses.