Design Centering and Yield Optimisation of MMIC's with Off-Chip Digital Controllers

F. Centurelli, R. Luzzi, G. Scotti, P. Tommasino, A. Trifiletti

Electronic Engineering Department, University of Rome "La Sapienza",
Via Eudossiana 18, I-00184, Roma, ITALY. Phone: +39 06 44585679, Fax: +39 06 4742647,
e-mail: trifiletti@die.uniroma1.it

In this paper, a new methodology to perform yield-oriented design of MMIC's in III-V technologies is proposed. A digital control of MMIC bias, based on process parameters estimation by on-chip auxiliary circuits, allows yield enhancement. The design centering approach and a distance-dependent correlated statistical model of HEMT devices are used to design the external controller. The design of a MMIC for optical digital systems has highlighted significant yield improvement with respect to previously proposed methodologies

INTRODUCTION

The development of microwave and millimetre-wave IC's requires very high performance technologies such as short gate III-V based ones. These technologies are often affected by a large dispersion of process parameters which results in circuit performance variability and can prevent the achievement of the desired yield. Yield and variability issues of an high performance IC have to be addressed in the performance optimisation design stage. High performance and high yield can hardly be guaranteed by means of standard MMIC design flows. Specific design methodologies in which statistical models of active devices are used jointly with yield optimisation techniques were presented by Krupenin et al (1), and by Kobayashi et al (2). These methodologies allow to obtain a good trade-off between performance and yield. Several approaches for statistical modelling of active devices in both linear and non linear operation, have been proposed by Meehan et al (3), Carrol et al (4), and Swidzinski and Chang (5), in order to perform circuit simulation within commercial CAD tools. In particular, a model in which correlation between parameters of devices on the same chip is accounted as a function of the distance among the devices themselves, has been recently developed by Centurelli et al (6). The yield optimisation problem has been addressed and analytically formulated by Director et al (7). Various approaches to find CAD-oriented design strategies have been proposed: in particular, the design centering was addressed in (3) and by Meehan and Purviance (8), the DOE by Carrol and Chang (9). Recently a novel yield optimisation strategy, based on the control of the MMIC bias performed by means of on-chip process parameters estimators and an external digital controller, has been presented by Scotti et al (10). In this paper, we propose a detailed design methodology which allows to determine the bias controlling function to be implemented into the digital controller, by analytically formulating the optimisation problem to be solved. The advantages of the new approach will be demonstrated from the viewpoint of design centering theory, which allows straight-forward comparison between the proposed method and previously published yield enhancement techniques.

YIELD OPTIMISATION APPROACHES

From a statistical point of view, the circuit yield Y is defined as the probability that the fabricated circuit shows an output response $G=[g_1, g_2, ..., g_n]$ (e.g. g_i are gain, return loss, noise figure, ...) comprised in a n-dimensional acceptability region A_G. In our approach the output response G is evaluated as a function of the parameters P=[X,V] which affect circuit performance, including both the noise factors X (i.e. the parameters which take into account of process dispersion and show large random variability) and the design factors V (i.e. parameters whose nominal values V_0 can be chosen by the designer in order to rise performance and yield). Each noise factor $x_i \in X$ can be considered as the sum of two statistically independent random variables:

$$x_i = x_{iSS} + x_{iLS} \qquad (1)$$

In Eq. (1) the first term represents the small-scale (on-chip) parameters variation and the second represents the large scale parameters variation. The standard deviation of x_i can be expressed as:

$$\sigma_T^{x_i} = \sigma_{SS}^{x_i} + \sigma_{LS}^{x_i} \qquad (2)$$

where $\sigma_{SS}^{x_i}$ takes into account of on-chip variability, and $\sigma_{LS}^{x_i}$ of large-scale variability (i.e. chip-to-chip, wafer-to-wafer, and run-to-run variability). A variability region $R_G(V_0, \sigma_T^X)$ is found for each set V_0 due to the random variation of noise factors X. The nominal values V_0 of the design parameters have to be chosen so that R_G is contained in the acceptability region A_G. Yield is maximised, under the hypothesis that no controlling scheme is imposed on the noise factors X, by solving the following optimisation problem:

$$\max_{V_O}\left\{Y = Prob\{G \in A_G\} = \int_{A_G} f_G(X, V_0, G)dG\right\} \qquad (3)$$

where $f_G(X,V_0,G)$ is the joint probability density function of the output response G(P). The expression in Eq. (3) shows that the yield can be enhanced by lowering the dimension of the variability region R_G and/or by changing the position of the variability region R_G with respect to A_G in order to maximise the overlapping region between high probability density parts of $R_G(V_0, \sigma_T^X)$ and A_G: this condition can be obtained by lowering parameter variations and/or the sensitivity of the circuit to parameter variations by an optimal choice of V_0. Some techniques have been proposed to enhance the yield by means of on-chip analogue bias regulators and/or feedback networks which allow to reduce the sensitivity of the circuit to noise factors. These techniques have proved to be efficient for certain topologies, leading to regulated current errors lower than ±3 % in presence of ±0.5 V threshold voltage variation as reported by Kobayashi et al (12). However, III-V technologies are not suitable to implement high gain and high precision operational amplifiers required to achieve bias control and stabilisation. Moreover, in complex circuits composed of DC-coupled amplifier stages, based on differential pairs and/or feedback-based topologies such as the transimpedance amplifier, regulation of the DC current of a certain number of devices may be a sub-optimal solution which is not able to guarantee the maximal yield. Recently, a technique has been proposed to estimate the values and control the effects of some noise factors by means of off-chip digital control loops (10): in the next section we focus on this technique by defining a procedure to achieve the optimal design of the bias control digital loop.

DEFINITION AND DESIGN OF THE CONTROL ARCHITECTURE

In the off-chip approach, a control circuit is used to perform both statistical parameter and/or temperature estimation (by means of on-chip circuits) and bias correction, in order to detect large-scale process parameters variation X_{LS} and to provide on-line correction to the fabricated circuit. The proposed control architecture is shown in Fig. 1: a set of N detectors, which allows variables estimation, is located on the MMIC chip, biased from the controlling chip. A critical step of the proposed procedure is to design variable estimators for a given statistical model: this issue has been addressed in (10). The estimated variables (i.e. a set of voltages and currents) are fed to the controlling chip (a low cost Si-based one) and converted into digital variables. For a given circuit, a matrix $M(X_{LS},B_I)$ is stored into a digital controller within the external chip containing, for a certain number of sets of values for the large-scale statistical variables X_{LS}, the optimal set of biasing voltages and currents B_I to be sent to the circuit in order to maximise both performance and yield. The procedure for the optimal design of the digital controller for a given MMIC is outlined as follows: the first step is to define the acceptability region A_G for the given design goals G; since the output response vector G depends on both the noise factors and the design factors, the second step is the identification of vectors X and V; the third step is the choice of the subset X_e of noise factors which can be estimated and the set of bias B_I (bias voltage of currents which affect X) to be used as controlling variables. This choice has to be done considering on one side the value of $\sigma_T^{x_i}$ and the impact of this variability on performance, and on the other side, the degree of controllability of each x_i as a function of the controlling variables. The next step requires to find the variability region for each of the estimated noise factors (this can be considered to be equal to the nominal value +/- 3 $\sigma_T^{x_i}$) and to divide it into n_i intervals.

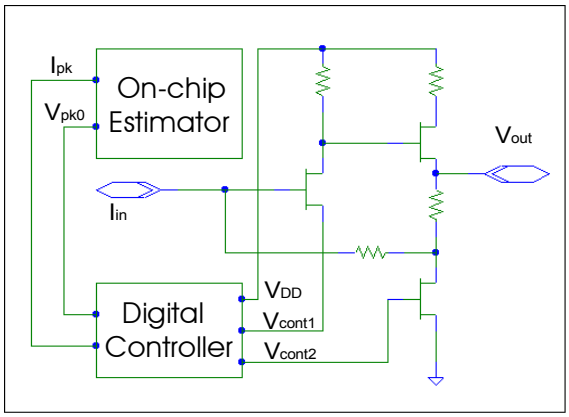

Figure 1: The designed MMIC with the external digital control

By following this approach in each of the n_i^N obtained regions, the following optimisation problem has to be solved in order to determine the optimum values of the biasing currents and voltages B_I for each estimated set X_e:

$$\max_{BI}\left\{ Y = \int_{A_G} f_G\left(X_e, X_{ne}, BI, V_o, G\right) dG \right\} \qquad (4)$$

where X_{ne} are the non-estimated noise factors, and in which only the small-scale portion of the standard deviation of the estimated variables ($\sigma_{SS}^{x_i} << \sigma_T^{x_i}$) has to be considered. The solution of the proposed optimisation problems requires a statistical model for the active devices: we propose to make use of the non linear statistical model presented in (6), in which variable partition in Eq. (1) is used for the statistical variables. By using this model, both on-chip dispersion and correlation as a function of the distance among the active devices are taken into account (including the effect of the distance between the estimation circuit devices and the operating devices) by means of the small-scale statistical model. Large-scale variations of the estimated variables are detected by the digital controller which is able to provide on-line correction to the fabricated circuit, provided that the matrix $M(X_{LS},B_I)$ is suitably loaded. It has to be noted that also for non-estimated factors X_{ne}, a large-scale statistical model would have to be used. However, a small-scale model can be used also for X_{ne} if the condition holds that large-scale process dispersion is mainly mapped into X_e parameters. In the optimisation problems defined in Eq. (4), the vector V_0 is the same at each iteration of the design process and is preliminarily found by means of the optimisation problem defined in Eq. (1), which is solved considering a small-scale variation for noise factors X_e and a fixed value of the vector B_I: the hypothesis holds that large-scale variations are cancelled by the off-chip controller. A greater yield can be achieved if each of the optimisation problems defined in Eq. (4) is changed into the following one:

$$\max_{V0}\left\{ \max_{BI}\left\{ Y = \int_{A_G} f_G\left(X_e, X_{ne}, BI, V_o, G\right) dG \right\} \right\} \qquad (5)$$

where the optimal set of biases B_I is found in each of the n_i^N regions, for each value of V_0 in order to avoid sub-optimal solutions. The yield optimisation problem defined in Eq. (4) or (5) highlights the advantages of the proposed technique: firstly, lower dispersion has to be considered during each optimisation for the estimated noise factors leading to a smaller variability region R_G; moreover, further degrees of freedom (the set of control/bias voltages and currents B_I) are introduced in each optimisation problem in order to increase the overlapping region between $R_G(V_0)$ and A_G. These considerations qualitatively show that a greater value for the overall yield can be found. The quantitative yield enhancement depends on the structure of the joint probability density function of the output response, and therefore is a function of the particular circuit under consideration.

Table 1
Simulated yield of the amplifier after nominal design, after design centering, and with the proposed methodology

Statistical parameters		Simulated Yield (%)		
ΔI_{pk} (% I_{pk})	$\Delta Vpk0$ (mV)	No Control	Design Centering	Ext. Control
-20	-0.5	0.2	3.6	16.6
-20	-0.3	13.8	51.2	63.6
-20	-0.1	48.2	35	78.6
-20	0	33.8	12	76.8
-20	0.1	10.4	2.8	73.4
-20	0.3	0	0	57.2
-20	0.5	0	0	10
0	-0.5	0	0	1
0	-0.3	0	9.6	41.6
0	-0.1	30.4	82.6	95.4
0	0	74.4	78.6	91.6
0	0.1	76.2	53.6	97.6
0	0.3	11.2	2.8	91.4
0	0.5	0	0	77.4
+20	-0.5	0	0	0
+20	-0.3	0	0	12
+20	-0.1	0.4	33	79.6
+20	0	13.4	85.6	96.4
+20	0.1	65.6	97.4	98.2
+20	0.3	79	47.6	98.4
+20	0.5	2	0	98.6
Average Yield		**21.9**	**28.4**	**64.5**

CASE STUDY

A transimpedance front-end amplifier (see Fig. 1) for 2.5 Gb/s digital optical communication system has been designed in PHILIPS PML D02AH GaAs p-HEMT technology within Agilent ADS CAD tool (11), using the statistical model presented in (6) which is able to take into account of the correlations among the device noise factors on the same chip. A nominal 54 dBΩ (50Ω loaded) transimpedance gain and a –3dB bandwidth of 1.8 GHz have been set as design goals. A minimum 53.5 dBΩ DC transimpedance gain and a minimum 50.5 dBΩ transimpedance gain at 1.8 GHz have been set as yield specifications to define the acceptability region. Large-scale variation has been supposed for parameters I_{pk} and V_{pk0} (3-σ equal to 20%·I_{pk} and 500mV, respectively), and the on-chip estimators proposed in (10) have been used. Yield optimisation results obtained by means of the proposed methodology have been compared to the design centering approach: results shown in Tab. 1 highlight significant yield improvement for the values of I_{pk} and

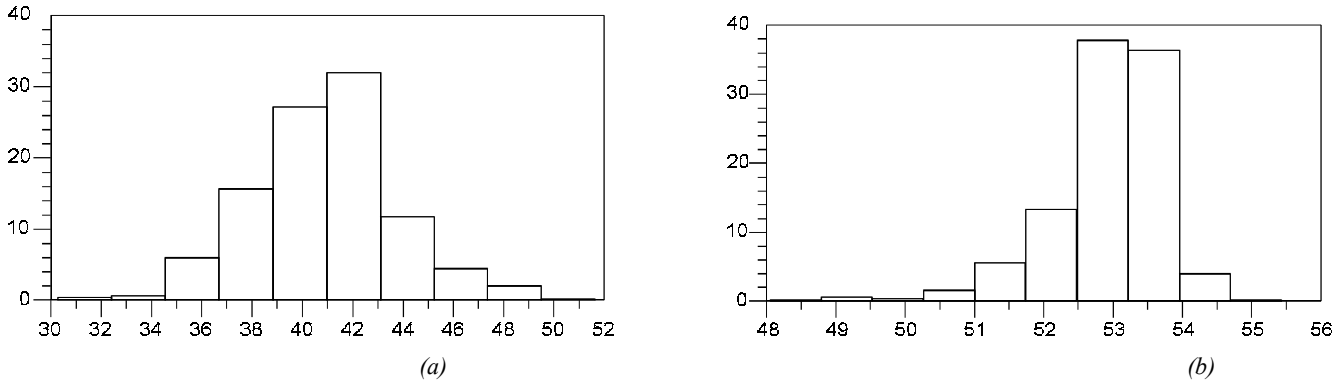

Figure 2: Simulated transimpedance gain at 1.8 GHz for ΔI_{pk} = +20% I_{pk} and ΔV_{pk} = 500mV:(a) with design centering, and (b) with digital controller

V_{pk0} comprised at the tail of the 3-σ region of the distribution, where the design centering is not able to guarantee acceptable yield values. In Fig. 2 the histogram which reports the percentage of occurrence obtained for the transimpedance gain at 1.8 GHz with a 500-iteration Monte Carlo analysis is shown for $\Delta I_{pk} = +20\% \cdot I_{pk}$ and ΔV_{pk0} = 500mV.

CONCLUSIONS

A methodology to perform yield optimisation of MMIC's by means of on-chip estimation of process parameter dispersion and off-chip digital control has been proposed. The procedure which allows to determine the bias controlling function to be implemented into the digital controller has been outlined, and the optimisation problems to be solved have been formulated. The advantages of the new approach have been demonstrated from the viewpoint of design centering theory which allows straight-forward comparison between the proposed method and previously published yield enhancement techniques.

REFERENCES

(1) S. Krupenin, R. R. Blanchard, M. H. Somerville, J. A. Del Alamo, K. G. Duh, P. C. Chao, *Physical Mechanisms Limiting the Manifacturing Uniformity of Millimeter-Wave InP HEMT*, IEEE Trans. Electron Devices, Vol 47 pp. 1560-65, Aug. 2000.

(2) K. W. Kobayashi, R. Esfandiari, B. L. Nelson, K. Minot, W. L. Jones, M. Biendenbender, R. Lai, K. L. Tan, J. Berenz, *Monolithic Regulated Self-Biased HEMT MMIC's*, IEEE Trans. Microwave Theory and Techniques," Vol. 42 pp. 2610-2616, Dec. 1994.

(3) M. D. Meehan, T. Wandinger, and D. A. Fisher, *Accurate Design Centering and Yield Prediction using the "Truth Model"*, Proc. IEEE MTT-S Digest, pp. 1201-1204, 1991.

(4) J. Carrol, K. Whelan, S. Prichett, and D. R. Bridges, *FET Statistical Modeling Using Parameter Orthogonalization*, IEEE Trans. Microwave Theory and Techniques, Vol. 44 pp. 47-54, Jan. 1996.

(5) J. F. Swidzinski and K. Chang, *Nonlinear Statistical Modeling and Yield Estimation Technique for Use in Monte Carlo Simulations*, IEEE Trans. Microwave Theory and Techniques 12, Vol. 48 pp. 2316-2324, Dec. 2000.

(6) F. Centurelli, A. Di Martino, P. Marietti, G. Scotti, P. Tommasino, A. Trifiletti, *A Non-Linear Statistical Model for GaAs FET Integrated Circuits*, GAAS 2002, European Gallium Arsenide and Other Semiconductors Application Symposium.

(7) S. W. Director, P. Feldmann, K. Krishna**,** *Statistical Integrated Circuit Design*, IEEE Journal of Solid-State Circuits, Vol. 28 pp. 193 –202, Mar. 1993.

(8) M. D. Meehan, J. Purviance*, Yield and Reliability in Microwave Circuit and System Design*, Artech House, 1993.

(9) J. Carrol and K. Chang, *Statistical Computer-Aided Design for Microwave Circuits*, IEEE Trans. Microwave Theory and Techniques, Vol. 44 pp. 24-32, Jan. 1996.

(10) G. Scotti, P. Tommasino, A. Trifiletti, *Bias Correction and Yield Optimisation of MMIC's with External Digital Control*, Microwave and Optical Technology Letters, Vol. 31 pp. 134-137, Oct. 2001.

(11) *Advanced Design System*, Agilent Technologies, 2001.

(12) K. W. Kobayashi, W. L. Jones, K. MacGowen, R. Kono, and L.-S. J. Lee, *A Monolithic DC Temperature Compensation Bias Scheme for Multistage HEMT Integrated Circuits*, IEEE Trans. Microwave Theory and Techniques, Vol. 44 pp. 261-268, Feb 1996.