HIGH FREQUENCY PROPERTIES OF Si/SiGe n-MODFETs: DEPENDENCE ON GATE LENGTH AND TEMPERATURE

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ABSTRACT

The HF performances of n-type strained Si channel Modulation Doped Field Effect Transistors (MODFETs) with 0.118 µm, 0.130 µm and 0.250 µm gate lengths are reported at 300 K and 50 K. At 300K, intrinsic cut-off frequencies f_{Ti} are 65 GHz, 58 GHz, 37 GHz and maximum oscillation frequencies f_{MAX} are 76 GHz ,60 GHz, and 100 GHz , respectively. The 0.130 µm device presents at 300 K a record intrinsic transconductance of 715 mS/mm and excellent noise performances with a de-embedded Minimum Noise Figure NF_{min} of 0.3 dB at 2.5 GHz. The variation of f_{MAX} underlines the importance of the device parasitic resistances.

INTRODUCTION

SiGe technology introduces band gap engineering and allows a flexible design of devices for RF applications. Si/SiGe based Heterostructure Field Effect Transistors (HFETs) or Modulation Doped Field Effect Transistors (MODFETs), respectively, with quantum well confinement appear to be well suited for high frequency performances [1,2] and have also promised excellent noise performances [3,4]. Moreover this kind of device is attractive due to their integration compatibility with the well established silicon technology [5]. The aim of this work is to present the experimental RF performances of n-channel SiGe MODFET when the gate length is reduced, the temperature is varied, and emphasizes the main parameters which can be further optimized to lead to enhanced device behavior.

EXPERIMENTAL

The epilayer structure of n-MODFETs is grown by solid source molecular beam epitaxy (MBE) on a high resistivity p-type Si substrate, starting with a relaxed SiGe buffer layer, the Ge content of which is graded from 0% to 45%. The core of the active structure is a 9 nm thick biaxially strained Si channel embedded between two $Si_{0.55}Ge_{0.45}$ undoped spacers and Sb doped carrier supply layers. The mushroom T-shaped Schottky gate is patterned by e-beam lithography. More details about device processing are given in [2].

On-wafer static and microwave measurements from 1 to 35 GHz with a HP8510C vector network analyzer were performed at 300 K and 50K. Static characterizations are limited towards low currents due to the coplanar probe leakage current (a few tens of nano Amps.) The extraction of the small-signal high-frequency electrical parameters of the MODFET uses an efficient and robust procedure based on an analytical formulation of the equivalent circuit [3].

RESULTS

Figure 1 shows the IV characteristics of a 0.13 µm gate-length (L_G) and 100µm width n-MODFET at 300K and 50 K. The main features are, the threshold voltage V_{TH} around 0 V for 300K and 50 K, the excellent saturation behavior, the small knee voltage < 0.6 V at 300 K as compared with Si-MOSFET's, the significant increase of current at 50 K which is over 60 % beyond saturation in the 0.2 V-0.5 V V_{GS} range. This clearly shows at low temperature the improvement of carrier mobility due to phonon absorption collapse and phonon emission reduction, and also the strong velocity overshoot effects in this 0.13 µm device. The control of carrier density by the gate voltage is increased at low temperature, as under these conditions, the carrier population in lowest sub-bands increases because the energy minimum of each band is lower and the sub-band energy rises [1]. The influence of deep level defects is not visible on the IV characteristics neither at 300 K nor at 50 K as it has often been observed in III-V HEMTs.

Turning to device RF characteristics we remark the importance of an adequate de-embedding (not shown) of the access transmission lines and contact pads in the case of 0.13 µm MODFET. The corrections amounts to 75 % of de-embedded cut-off frequency f_T and to 50 % of maximum frequency of oscillation f_{MAX}. They are due to significant losses of the SiGe buffer and also of the Si substrate.

Figure 2 illustrates the strong increase of f_{MAX} for different gate lengths as a function of V_{GS} at 300K and 50K. The variations of f_{MAX} , and of f_T (not shown here) illustrate the bias range dependence of the devices on the epilayer structure (doping level, layer thickness). The strongest increase of f_{MAX} at 50 K is obtained for 0.25µm. It underlines the importance of having small access resistances particularly R_S and R_G which are smaller for the 0.25 µm than for the other devices (table 1). Therefore a self aligned technology will be beneficial at gate-lengths ≤ 0.15 µm.

Figure 3 shows the intrinsic transconductance g_m for a 0.130 µm and a 0.250 µm device as a function of the intrinsic drain voltage $V_{DS} - I_{DS} \cdot (R_S + R_D)$ for V_{GS} corresponding to maximum transconductance g_{mmax}. For the 0.130 µm device a g_{mmax} = 715 mS/mm is reached at 0.5 V drain voltage and 300K. It rises to 874mS/mm at 50K. To our knowledge, these values are the highest transconductance values reported so far for SiGe heteroFETs at 300K and 50K. We underline that the maximum gain is attained at low drain bias current, which is favorable in low power mobile communication applications.

Figure 4 illustrates the intrinsic and the extrinsic delay times t_i and t versus $1/L_G$ at 300K and 50 K, where $t_i = 1/(2\pi f_{Ti})$ and $t = 1/(2\pi f_T)$. We point out the significant improvement of f_{Ti} at low temperature. At 300K the difference between f_T and f_{Ti} increases at shorter gate lengths as a consequence of higher parasitic resistances (Table 1). As temperature is lowered, the f_T and f_{Ti} improvement are 60 % and 52 % for 0.13 µm gate length transistor, 65% and 84% for 0.25 µm, respectively. The drastic improvement for 0.25 µm device can be attributed to lower values of R_G and R_S. Noise measurements of 0.13 µm gate length device have shown excellent low noise performances with a minimum noise figure NF_{min} of 0.3 dB at 2.5 GHz for V_{DS} = 1.25V and I_{DS} = 7.7 mA. At low temperature, the increase of g_m and f_T and the reduction of parasitic resitances leads to estimate a NF_{min} = 0.05 dB which is smaller than measurements uncertainties.

CONCLUSION

High frequency performances at 300K and 50K of Si/SiGe n-MODFET's with different gate lengths have been presented. They show the high intrinsic f_{Ti} and g_m which can be obtained at very low drain voltage and power dissipation and the increase of these parameters at reduced gate-length. Very low noise has also been measured for the 0.13µm MODFET. The temperature analysis at 300K and 50K gives clear directions of optimization for further performance improvements

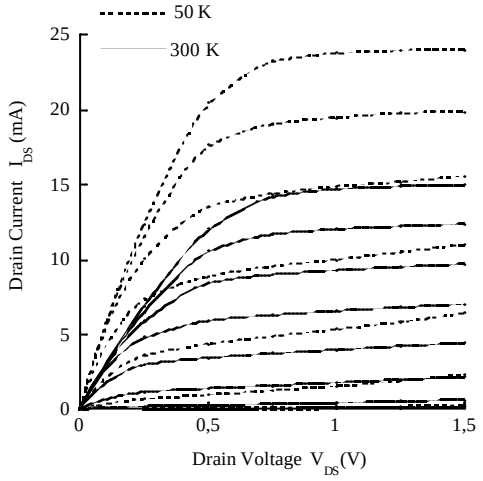

Figure 1. I-V characteristic of a SiGe 0.13 µm n-MODFET. Solid lines 300 K, dashed lines 50K. V_{GS} sweep is from -0.2 V up to +0.5 V by step of +0.1 V.

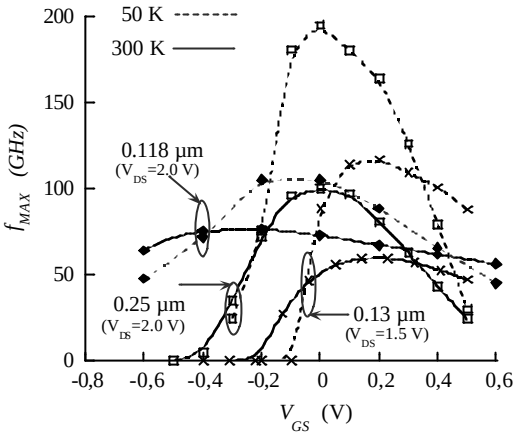

Figure 2. f_{MAX} for n-MODFET versus gate voltage V_{GS} for different gate lengths at 300K (solid lines) and 50 K (dashed lines), squares 0.250 µm, crosses 0.130 µm, diamonds 118µm

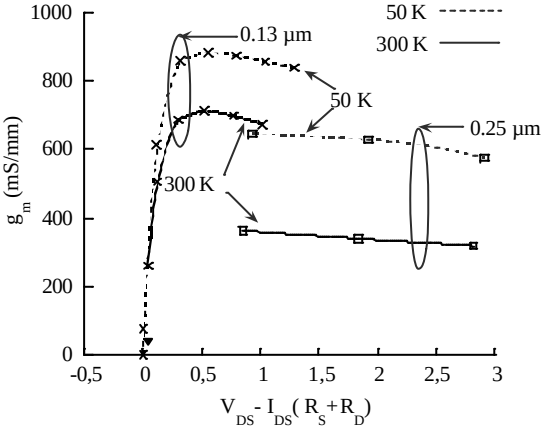

Figure 3. Intrinsic transconductance versus intrinsic drain voltage for two gate lengths at 300K (solid lines) and 50 K (dashed lines), squares 0.25µm device , crosses 0.13 µm device.

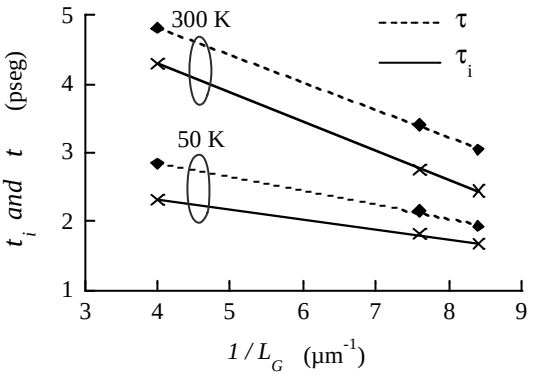

Figure 4. Intrinsic and extrinsic delay times t_i and t versus $1/L_G$ at 300 K and 50 K

Temp (K)	Gate Length (μm)	R_G (Ω/mm)	R_S (Ω-mm)	R_D (Ω-mm)
300	0.118	14.50	1.900	0.530
	0.130	75.00	1.200	2.100
	0.250	83.25	0.240	0.900
50	0.118	5.1	0.560	0.600
	0.130	38.80	0.497	0.883
	0.250	39.96	0.186	0.396

Table 1. Parasitic access resistances for the SiGe n-MODFET's for different gate lengths and partly different device layouts at 300K and 50K.

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