

CORRELATION BETWEEN THE RELIABILITY OF HEMT DEVICES AND THAT OF A COMBINED OSCILLATOR-AMPLIFIER MMIC

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ABSTRACT

We evaluate an oscillator-amplifier MMIC submitted to high-temperature operating life time tests. To relate adequately these results with individual components' results, it is important to realise that failure mechanisms in non-linear MMICs are governed by the maximally instantaneous voltages/currents and hence that comparisons should be conducted at equal instantaneous conditions.

INTRODUCTION

The microwave and millimetre wave market for circuits and systems based on GaAs pHEMTs is steadily growing. An important aspect for MMICs to be inserted in commercial applications is reliability. To evaluate the reliability of the GaAs pHEMT MMIC technology, we have designed and fabricated a combined oscillator-amplifier MMIC and submitted this circuit to high temperature operating life time tests. These stress test results will be related to the reliability of the circuit's individual components.

DESIGN AND RELIABILITY OF THE OSCILLATOR-AMPLIFIER MMIC

Circuit design

The test vehicle used to evaluate the reliability of the GaAs pHEMT MMIC technology is a 5 GHz microstrip combined oscillator-amplifier. We choose the topology of an oscillator followed by a buffer amplifier, because in this way the amplifier is RF stressed by the oscillator as soon as DC bias is applied. Hence, RF stress test conditions are obtained, whereas only a DC bias has to be applied to the MMIC located in the furnace during the life time tests. The oscillation frequency (5 GHz) is relatively low considering that GaAs pHEMTs are the active devices. The reason is that we also want to study the possible degradation of the typical lumped passive components in an MMIC technology.

In general, an oscillator consists of a negative resistance and a resonator. The negative resistance is principally obtained by destabilising the pHEMT at the desired oscillation frequency. As resonator, we choose an on-chip lumped element based configuration, despite its low Q compared to off-chip resonators, because it is the purpose to evaluate the reliability of the pHEMT MMIC technology and not that of possible external components. The actual oscillation frequency is determined by the parallel resonant circuit formed by the input capacitance ($C_{gs}+C_{gd}$) of the HEMT in the oscillator subcircuit and a spiral inductor. We added a MIM capacitor in parallel to the transistor's gate to minimise the sensitivity of the oscillation frequency to processing variations. The widths of the HEMTs in the oscillator and amplifier subcircuits are 50 μm and 100 μm , respectively. Because a robust design was required for the envisaged reliability tests, parallel feedback is used in the amplifier topology to ensure broadband stabilisation. The non-linear GaAs pHEMT model used in both the oscillator and amplifier designs is an in-house developed look-up table model (1). A picture of the oscillator-amplifier MMIC is shown in Figure 1. The design is compact (1.5 mm x 1.2 mm), because the bias networks act simultaneously as matching circuits. The output power is 3 dBm, while the higher order harmonics are suppressed with more than 30 dB.

Reliability test preparation

The fabricated oscillator-amplifier MMICs have to be properly prepared for the reliability tests. The MMIC needs to be packaged to prevent any contamination with air. The package has to be put on an MIC carrier to facilitate DC biasing during the stress test and to enable RF measurements at regular time points. It is also necessary to have a test-fixture that is compatible with the MIC carrier to perform calibrated RF measurements.

After finishing the processing, the wafers are tested for DC and RF functionality. Consequently, the wafers are diced and the individual chips are mounted into a ceramic Kyocera package by using a conductive glue (preform $\text{Au}_{0.80}\text{Sn}_{0.20}$). To avoid low frequency oscillations, chip capacitors are put in the package as close as possible to the DC bonding pads. The wire bond connecting the oscillator RF output to the feed-line of the package has to be as short as possible to minimise its inductive effect on the MMIC performance. The package is mounted on an alumina carrier by conductive glue. Supplementary bias networks are added off-chip to enhance the circuit's stability in the kHz and MHz frequency bands. After verifying the DC functionality, the package is hermetically sealed. Figure 2 shows the picture of a package containing

two oscillator chips and corresponding bias circuitry, that is mounted on the alumina substrate. All the additional SMD and chip components must be well suited to the thermal environment. Therefore, we tested the SMD capacitors separately in the furnace at the considered temperatures. No degradation was noticed after 1000 hours. The alumina substrate is realised in coplanar waveguide technology, which prevents the processing of via holes. Furthermore, a better ground connection between the package and the MIC carrier is guaranteed due to the absence of the inductive contribution of the via holes. Finally, in order to perform RF measurements, the MIC carrier can be mounted in a test-fixture, that provides a transition between the coplanar waveguide alumina MIC and a coaxial SMA connector.

High temperature operating life time test

The mounted MMICs are submitted to a high temperature operating life time test. The furnace temperature is $T_{amb} = 175^\circ\text{C}$ and the number of circuits for this test is 9. At regular time points, the DC characteristics of the HEMTs of both sub-circuits are measured. Also the output power and the oscillation frequency are monitored. The most dominant change during the test is a decreased threshold voltage V_T . The order of the V_T decrease, which is about -80 mV, is the same for both the oscillator HEMT (Figure 3) and the amplifier HEMT. The drain-source current I_{ds} and the transconductance g_m in the linear region decrease slightly ($\approx 7\%$), which can be attributed mainly to the V_T decrease. The V_T decrease is accompanied by a decrease in the input capacitance, which results in an increase in the oscillation frequency, as is shown in Figure 4. The variation on this shift, which is between 4 MHz and 70 MHz, is rather large. One can compare this to the variation of the oscillation frequency when the gate-source voltage V_{gs} of the oscillator HEMT is varied at room temperature by the same amount, which corresponds to 10 MHz. The difference between these shifts can be explained by the fact that during the reliability test also the g_m and the input capacitance of the amplifier HEMT change and hence the load presented to the output of the oscillator is modified. We will try to explain the physical cause of the V_T decrease in the next Section, by correlating these circuit reliability results under high temperature RF operating conditions with the reliability results of the constituting components and especially the GaAs pHEMTs.

RELIABILITY OF THE INDIVIDUAL COMPONENTS

In order to clarify the changes of the oscillator performance as function of stress time, it is necessary to examine the reliability of its constituting elements. First, we shortly focus on the passive components, before we examine three tests performed on the active devices. The first test done on the GaAs pHEMTs is a high temperature operating life time test, where a DC bias has been applied to the devices in the furnace. The second test is a high temperature storage test, where no DC bias is applied. The third test involves an operating life time test at room temperature.

Reliability of passive components

The passive components present in the investigated MMIC are microstrip lines, air bridges, spiral inductors, an active layer resistor, MIM capacitors and via-holes. We did not explicitly perform reliability tests on these passive components, but estimated their possible degradation based on the well covered analyses available in literature (2,3). In this way, it is determined that dielectric breakdown in the MIM capacitors is very unlikely to happen, because all voltage levels in the investigated MMIC are relatively low. Also, we do not expect that electromigration will happen in the microstrip lines, spiral inductors and airbridges, because the nominal current density is less than 40 % of the critical current density for electromigration. Electromigration will also not be present in the active layer resistor, because no DC current is flowing through the resistor. However, the resistance value may shift due to ohmic contact degradation. A resistance shift in the via holes may be noticed due to differential thermal expansion. This will result in a reduced DC current.

High temperature operating life time test on GaAs pHEMTs

The high temperature operating life time test has been performed on passivated GaAs pHEMTs. After wafer dicing, the single devices are packaged and hermetically sealed in TO18 packages. The furnace has a dry nitrogen atmosphere to avoid lead oxidation and/or contamination. Since the long DC wires by which the DC bias is applied can cause low-frequency oscillations, an SMD capacitor is put between the gate and the source leads. The furnace temperature T_{amb} is 175°C and the devices are biased for normal amplifier operation. The DC V_{gs} is kept fixed on 0 V and the DC drain-source voltage V_{ds} is adjusted to obtain a DC I_{ds} equal to 200 mA/mm. During the tests, the gate-source current I_{gs} and I_{ds} changes are monitored in situ and DC measurements at room temperature are performed at intermediate time points.

Figure 5 shows the change of V_T in the linear region. During the first days, we notice a slight negative V_T shift, which is probably related to thermal enhanced electron trapping (4). After about 100 hours, another failure mechanism becomes apparent since the V_T becomes more positive. It is gate sinking, which is related to the Schottky gate contact degradation (5,6). The gate contact of the studied technology consists of Ti(50 nm)/Pt(50 nm)/Au(350 nm). The gate sinking effect could be minimised by using Mo or WSi as the barrier material (7), but it has to be noted that the shown tests were performed on a standard GaAs pHEMT technology where no special technology modifications were yet done with regard to reliability improvement. At $T_{amb} = 175^\circ\text{C}$, the positive shift of V_T is about 45 mV. This becomes 110 mV in case of a similar test performed at $T_{amb} = 220^\circ\text{C}$. The I_{ds} decreases by about 2.4 mA/mm, which can

be caused by an increase of the channel resistance and/or the ohmic source and drain resistances. The increase of the open channel resistance is expected when gate sinking occurs (2). The second possible reason for the I_{ds} decrease could be ohmic contact degradation. However, it has been reported (2) that degradation of the used type of ohmic contacts (AuGe(120 nm)/Ni(15 nm)/Au(60 nm)) only becomes dominant at a temperature higher than 200°C.

As an intermediate conclusion, we can state that there is no direct correlation between the dominant failure mechanism of the oscillator-amplifier MMIC and the case where single HEMTs are DC stressed at conditions of amplifier operation, because the sign of the V_T shift is opposite.

High temperature storage test on GaAs pHEMTs

The high temperature storage test has been performed at a furnace temperature of $T_{amb} = 220^\circ\text{C}$ on 11 packaged GaAs pHEMTs. Figure 6 shows the behaviour of V_T as function of stress time. The V_T decreases about 110 mV. A negative shift of V_T can be explained by positive charge under the gate. This positive charge can be created by the thermal activated process to trap electrons. Similar negative V_T shifts in GaAs pHEMTs at high temperature storage test conditions have been reported (4). This physical phenomenon is normally accompanied by an increase in I_{ds} , whereas we measured a decrease of I_{ds} as function of time. This decrease of I_{ds} can be explained by a second failure mechanism that is active at these stress conditions, which is ohmic contact degradation.

We notice here a similar behaviour as in the case of the oscillator-amplifier MMIC, namely a negative V_T shift. However, it is our opinion that this thermal activated process is not the dominant failure mechanism in the MMIC case. A reason is that we estimated from separate tests that the channel temperature of the devices during the oscillator stress tests is not much higher than the ambient temperature.

Operating life time test at room temperature on GaAs pHEMTs

The previously described reliability tests were all thermal tests. In this paragraph, electrical stress tests at room temperature will be discussed. In a previous study (8), the effect of hot electron stress was studied on the same GaAs pHEMT technology. The change in device performance was evaluated by DC and RF characterising the samples before and after 60 min. stress at $V_{gs} = 0$ V and $V_{ds} = 5.5$ V. This test introduced a negative V_T shift by about 60 to 70 mV. This decrease is caused by a build-up of positive charge underneath the gate. The positive charge accumulation is likely due to deep traps capturing holes generated by impact ionisation and flowing towards the gate.

Our opinion is that the physical cause of the V_T decrease during the oscillator stress test is most probably due to impact ionisation. The measured output power of the MMIC is about 3 dBm. Since the MMIC output was left open (unloaded) while the circuit was located in the furnace, the maximal AC drain voltage is doubled compared to the 50 Ω case, and hence impact ionisation conditions are temporarily reached during the RF cycle.

CONCLUSIONS

We have investigated the results of a high temperature operating life time test on a non-linear MMIC, being a combined oscillator-amplifier. To clarify the observations, we examined the reliability of the constituting components and especially the GaAs pHEMTs. By conducting and analysing several stress tests on these active elements, we showed that the most dominant failure mechanism happening in the studied MMIC is impact ionisation.

These experiments are a good illustration of the conclusion that the failure mechanisms occurring in a non-linear MMIC are governed by the maximally instantaneous voltages/currents and hence that comparisons with other reliability tests should be conducted at equal instantaneous conditions.

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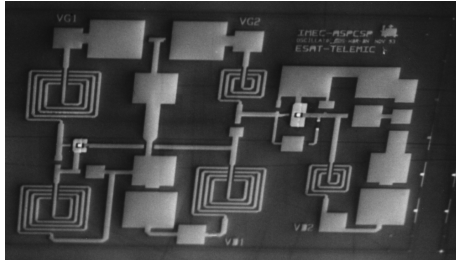


Figure 1: SEM picture of the osc-amp MMIC (1.5 mm x 1.2 mm), taken after c-gate metallisation.

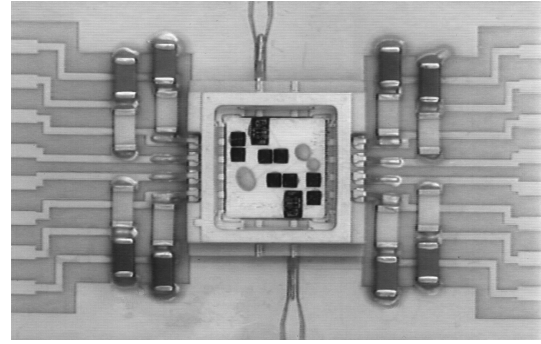


Figure 2: Overview picture of the MIC containing 2 packaged oscillators and DC bias networks.

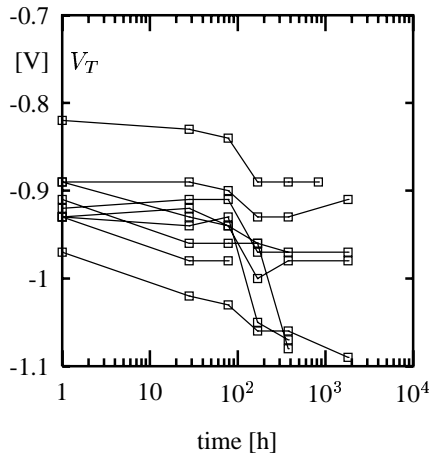


Figure 3: V_T measured at $V_{ds} = 20$ mV versus stress time of the GaAs pHEMT in the osc. subcircuit.

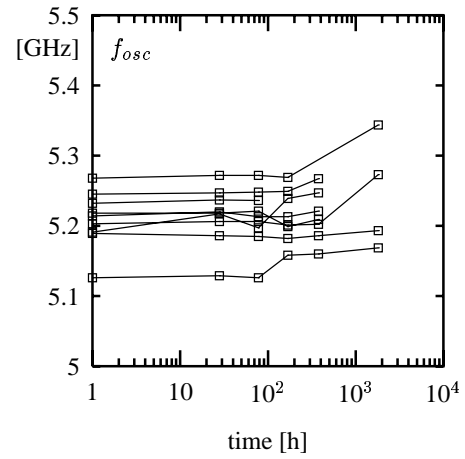


Figure 4: Oscillation frequency f_{osc} versus stress time of the GaAs pHEMT based MMIC oscillator.

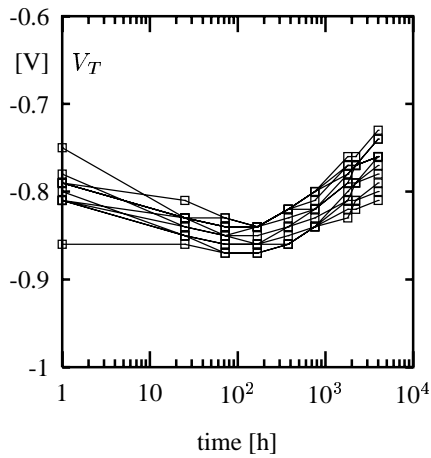


Figure 5: V_T measured at $V_{ds} = 20$ mV versus time of 100 μm GaAs pHEMTs ($T_{amb} = 175^\circ\text{C}$).

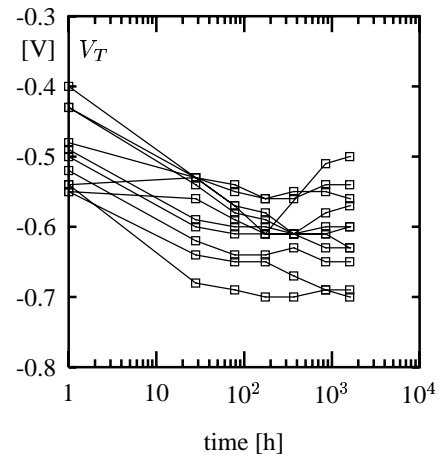


Figure 6: V_T measured at $V_{ds} = 20$ mV versus time of 100 μm GaAs pHEMTs ($T_{amb} = 220^\circ\text{C}$).