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QUASI-MONOLITHIC INTEGRATION TECHNOLOGY (QMIT) FOR POWER APPLICATIONS

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ABSTRACT

In this paper, we address the most important issues related to realisation of μ-wave and mm-wave circuits containing power devices in the novel technology of Quasi-Monolithic Integration Technology (QMIT). A finite element simulator (2D and 3D), a scanning probe microscopy (SPM), a nanometer surface profiler (DEKTAK) and a Peltier element (PE) have been used to optimise the standard structure of QMIT with respect to these issues and limitations in fabrication process.

The first important issue is the thermal resistance of QMIT structure. Using a 2D finite element method, the effects of the most important parameters on thermal resistance such as the distance between active device and substrate (W), the thermal conductivity of glue (k_{epoxy}) and use of a heat spreader to decrease thermal resistance have been investigated in detail.

The second important issue is the induced thermal stress in QMIT structure which results from differences in thermal expansion coefficient of materials involved. A 3D finite element simulator, a scanning probe microscopy (SPM) measurements and a nanometer surface profiler (DEKTAK) accompanied with a Peltier element (PE) have been used to simulate and measure the thermal stress distribution in QMIT standard structure. Then, the effect of the most important parameters such as W, baking temperature of epoxy and material properties of epoxy have been described in detail.

INTRODUCTION

Quasi-Monolithic Integration (QMI) technology is a new alternative to monolithic circuit fabrication for microwave and millimetre wave integrated circuits ([1] - [4]). In this technology commercial devices such as microwave FETs are embedded in a micromachined low cost high resistivity silicon substrate on which the passive circuit is fabricated. Interconnects between the active devices and passive components are realised using air bridge technology [2].

This technology allows the fabrication of planar high frequency circuits which exhibit advantages of both MMICs and hybrids. The use of micromachining and thin film technology ensures fabrication of reproducible interconnects with very low parasitic inductance and capacitance. Passive devices, which usually require large chip areas, are fabricated on a low cost high resistivity silicon substrate using coplanar techniques. Other advantages of this technology are the possibility of batch processing, the use of active devices from different technologies and having a thermal resistance comparable to that of standard MMICs with a thick Si-substrate ([2] - [5]).

For low power devices, QMI technology has been tested and it has shown good results ([3] - [4]). In the next step, we are trying to optimise this technology for fabrication of microwave and millimetre wave circuits containing power devices. In such circuits, one of the main problem is heat transfer to the environment and another one is the stress induced by differences in thermal expansion coefficient of materials involved. The induced thermal stress not only effects the reliability and life time of packaging but also affects the electrical characteristics of the active devices used, which is crucial for microwave and mm-wave design.

EFFECTS OF DIFFERENT PARAMETERS ON THERMAL RESISTANCE

In this section, effects of different parameters such as width of epoxy (distance between active device and Si substrate), thermal conductivity of epoxy and heat spreader in the back side of the wafer are described. The model used, boundary conditions and properties of materials involved are discussed in [5].

A. Effect of epoxy (W and k_{epoxy}) in the standard structure

As shown in Fig. 1 the distance between the active device and the substrate is W. In the technology process steps, W is limited to maximum value of 20 μm otherwise the air-bridges become susceptible to breakage. Fig. 2 shows the total thermal resistance for W equal to 5, 10 and 20 μm. As expected, thermal resistance decreases with decreasing W. Fig. 3 shows simulation results for W= 5 μm and k_{epoxy} equal to 1, 2, 3, 4 and 5 W/mK. Thermal resistance decreases with increasing k_{epoxy} but even for the best case, k_{epoxy} = 5 W/mK and W = 5 μm, thermal resistance is high.

B. Effect of heat spreader in the standard structure

The best thermal conductive epoxies have a poor thermal conductivity, so that in the QMIT structure thermal resistance is high. It is possible to fill out the hole at the backside of the substrate a with heat spreader (desired material) and decrease thermal resistance to values comparable to those in MMICs. Fig. 4 shows the results for different thermal conductivity of the heat spreader and W of 20 μm. As is shown, with the gold backside heat spreader, the thermal resistance of 10.85 [°C/W] is attained which is adequate for power applications.

EFFECTS OF DIFFERENT PARAMETERS ON THE THERMAL STRESS

In this approach, it is assumed that at the beginning of the baking process, the glue is fluid and expanded. The glue is baked in this state. Due to different thermal expansion coefficients of Si, GaAs and glue, stress builds up when the structure is removed from the oven (at room temperature). Normally the baking process of the epoxy is done at different temperatures. Because the Young's modulus of the epoxy at temperatures higher than the glass temperature is much smaller than that at lower temperature, we have assumed that at these temperatures, the stress is very low and most of the stress is induced by the temperature difference between the glass temperature and operating temperature. In this method the stress created is determined by measuring and mapping the surface profile of Si-wafer around the embedded devices using DEKTAK and SPM. In this summary because of limited pages the SPM measurements and most of the simulation results are not shown.

A. Effect of baking temperature of epoxy and power dissipation of the active device

According to the manufacturer's data sheet [6] minimum baking temperature of the epoxy may vary from 50 °C for 12 hours to 100 °C for 20 min. For baking temperatures of below Tg, the temperature difference (DT) is equal to the difference between room temperature (RT) and baking temperature. For the baking temperatures higher than Tg, DT is equal to the difference between Tg and RT.

Using the thermal resistance of QMIT structure, the power dissipation in active device can be easily related to DT. The thermal resistance for different structure of QMIT has been simulated and optimised [5]. The results can be used to have the thermal stress distribution as a function of power dissipation of active device and these results are not only required to investigate the reliability and life time of the packaging but also are useful for characterisation and modelling of the active device, which is very important in μ-wave and mm-wave design. The measurement results for DT equal to -74.5 °C, -54.5 °C, -34.5 °C, -14.5 °C with DEKTAK are compared with the simulation results in Fig. 5 and a good agreement between them is achieved.

B. Effect of elastic properties of epoxy

Calculated maximum "von Mises" thermal stress for the standard QMIT structure as function of Young's modulus of epoxy is presented in Fig. 6. In these simulations, W is 20 μm and DT is -74.5 °C. As shown, the lower Young's modulus of the epoxy is, the lower is the thermal stress but also the mechanical strength. On the other hand, some other parameters such as thermal conductivity, thermal expansion coefficient and permeability near to those of Si and GaAs should be considered and use a trade off among them.

C. Effect of different geometry of epoxy

Fig. 7 shows the calculated maximum "von Mises" thermal stress as a function of W. In the fabrication process, the minimum of W is about 10 μm and is determined by the defects in the cutting process of the

active device which is done by the manufacturer but the maximum of W is determined by the thermal stress and corresponding displacement result from the DT in the next fabrication steps. A large of displacement breaks the air bridges in the next steps. From the Fig. 7 the optimum W is between 10 µm to 15 µm.

OPTIMISATION OF QMIT

According to Fig. 4, electroplated gold backside heat spreader is a good solution for a low thermal resistance.

Optimum W with respect to maximum thermal stress is between 10 µm and 15 µm. The effect of W for thermal resistance can be ignored as long as a high thermal conductivity backside heat spreader is used. Minimum dimension of W is determined by the defects in active devices related to their dicing process by the manufacturer and is equal to 10 µm. We elected a W of 10 µm to 15 µm which is practically possible. The epoxy should be electrically non-conductive but of a high thermal conductivity. Considering fabrication process and availability, an epoxy with thermal conductivity of 1.1 W/m.K is used which has a proper Young's modulus of 0.8 GPa.

Lower baking temperatures give lower induced thermal stress. The baking process can be performed in a shorter time at a higher baking temperature or longer time with lower temperature. We have used a low baking temperature of 60 °C (DT = -34.5 °C) and a long baking time of 12 hours.

CONCLUSION

Geometry, properties of materials involved and fabrication process of the QMIT for power applications have been optimised, considering practical limitations in the fabrication process. 2D static heat transfer and 3D thermal stress simulations accompanied with SPM and DEKTAK measurements have been used. Remarkable agreement between calculated and measured displacements created by thermal stress was found.

REFERENCES

[1] E. Wasige, et al. "Air Bridge Based Planar Hybrid Technology for Microwave and Millimeter wave Applications", *IEEE MTT-S Int. Microwave symp. Dig.*, pp. 925 - 928, June 1997.

[2] -----: "12 GHz Coplanar Quasi-Monolithic Oscillator", *IEEE MTT-S Int. Microwave Symp. Dig.*, Paper MO3B-5, June 1999.

[3] -----: "GaAs FET Characterisation in a Quasi-Monolithic Si environment", *IEEE MTT-S Int. Microwave Symp. Dig.*, Paper THF5-5, June 1999.

[4] G. Kompa, E. Wasige, and M. Joodaki, "Quasi Monolithic Hybrid Technology Based on Si Micro-machining and Low-Temperature Thin-Film Processing", *World Micro-technologies Congress of MICRO-TEC.2000*, pp. 109-114, Sept. 2000.

[5] M. Joodaki, et al. : "Static Thermal Design of Quasi-Monolithic Integrated Technology (QMIT)", *8th IEEE Int. Symp. on Electron Devices for Microwave and Optoelectronic Applications EDMO2000*, pp. 117-122, Nov. 2000.

[6] Epoxy Technology Inc.: "Data sheet of EPO-TEK HF74.

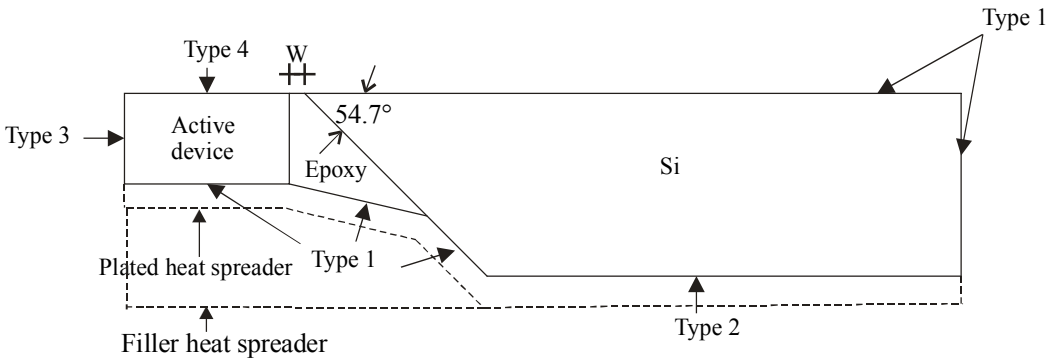

Fig. 1 Half of the standard structure of QMIT.

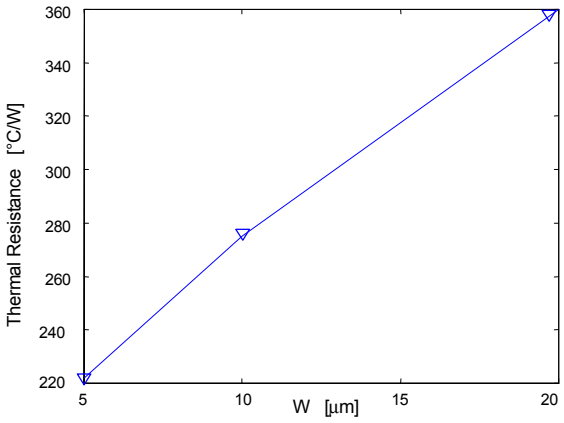

Fig. 2 Total thermal resistance for W= 5, 10 and 20 µm in the standard structure of QMIT

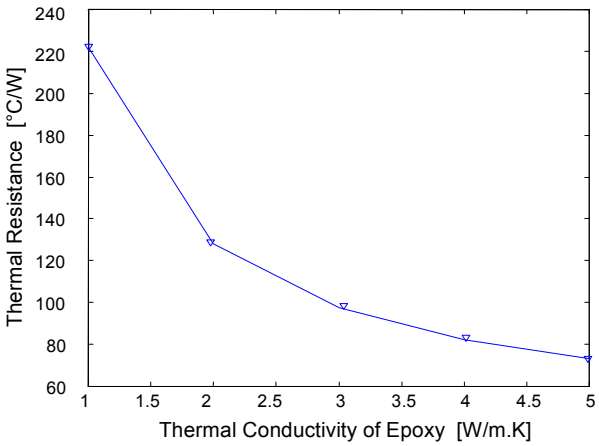

Fig. 3 Total thermal resistance for W = 5 and k_{epoxy} = 1-5 W/mK in the standard structure of QMIT.

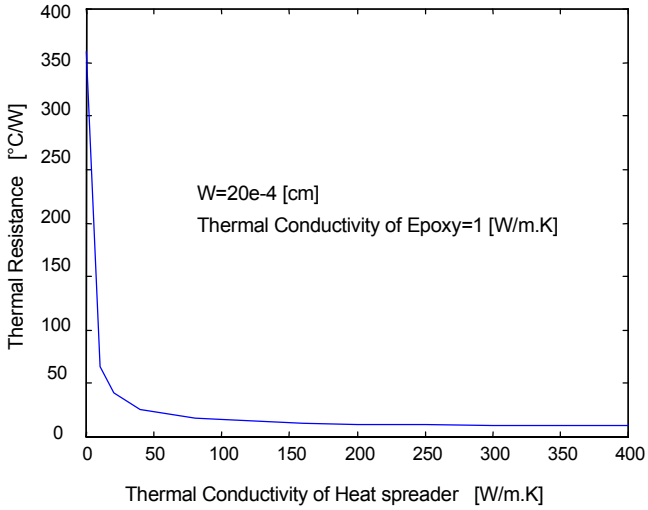

Fig. 4 Total thermal resistance as a function of backside heat spreader thermal conductivity.

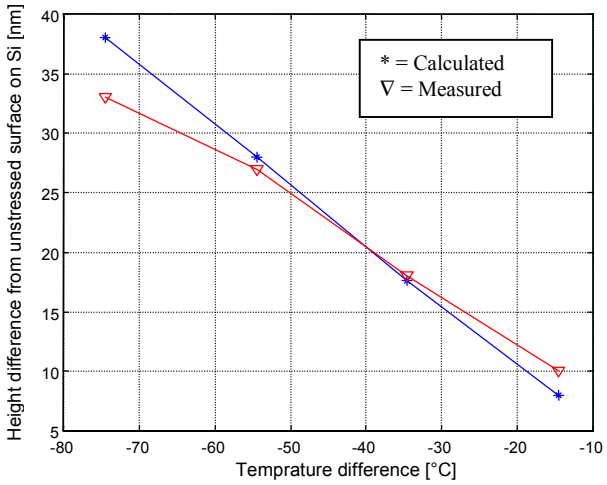

Fig. 5 Measured and calculated maximum height difference from the unstressed surface on Si-wafer in A-A direction.

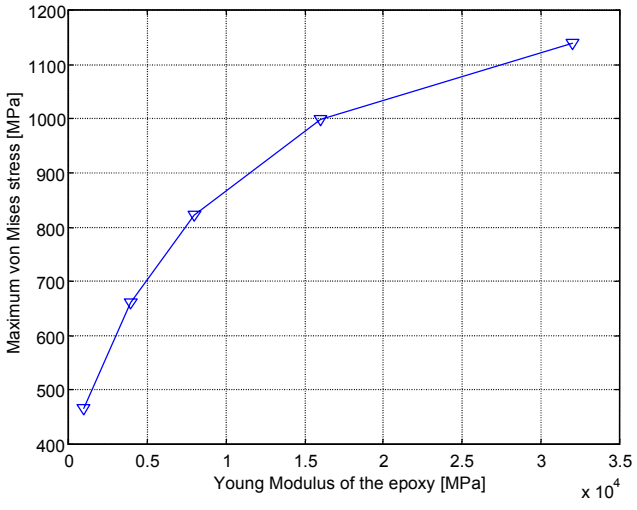

Fig. 6 Maximum "von Mises" stress as a function of the epoxy Young's modulus. W = 20 µm and DT = -74.5 °C.

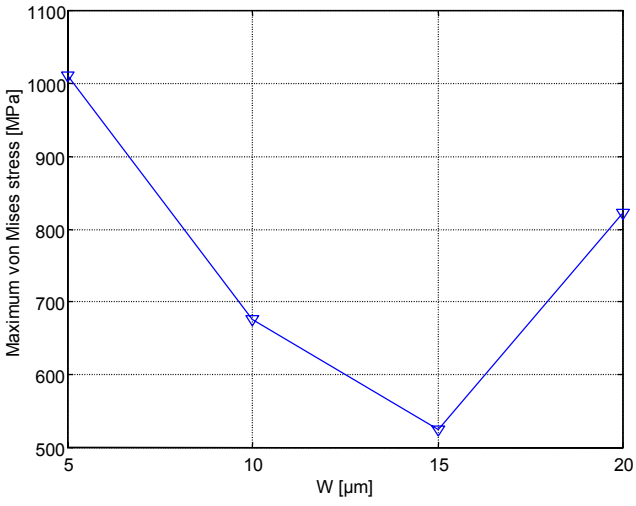

Fig. 7 Maximum "von Mises" stress as a function of W.