High Power HBT Technologies : Present and Trends

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Abstract

The HBT technology is now mature and offers a great variety of RF products for telecom applications, specially power amplifiers for which a high level of linearity is requested. The reliability has been the limiting factor in the supplying of high power amplifiers and nowadays only medium HPA are available in catalogue. Also, regarding the huge quantities of papers published in the mid 90s relating the interest of this technology for high PAE / Power, very few of the competitors have been successful. In Europe, open foundry services are available through UMS for high power applications ranging up to Ku band. New advances in term of thermal management / electrical behaviour and topology have been pushed ahead tending towards the limit of high power density. An improved version is underway to set up a doubling of the output power by cell (2.5W in X- Band). To address the market of the base stations, very high power transistors have been designed. Also, the Collector-Up DHBT offer potential improvement in term of high power at high frequency (1W at 40 GHz).

I. Introduction

Extensive efforts have been done in the past to push the limits of InGaP/Gas HBT technology towards very high power density.
A lot of papers were published, exhibiting impressive results in term of power, power density and efficiency. These work focus mainly for applications operating in X band applied to T/R module. At this time, the HBT was the most competitive solution face to HFET or PHEMT power technologies.
High reliability levels required by these applications put a serious challenge to manufacturers and many of them stopped their developments. Today, many suppliers propose circuits or open foundries based on HBT technology addressing wireless applications for which low cost / high volume is required. The InGaP/GaAs system is used as emitter in the greater part due to his superior behaviour in term of reliability. But the counterpart to his situation, is that these technologies are used for medium power applications (below 30 dBm) in which high linearity associated to the best efficiency is sought. Furthermore, many of them are limited to L band applications and exhibit typically a MTBF close to 10^6 hours at 150°C.
Advanced researches have been lead to overcome the reliability limitations through own R&D plans and research programs funded by the EC [1]. These work got impressive results and since the year 2000, open foundry services could be used for high power / high efficiency applications up to Ku band [2]. HBT technology is very suited to deliver high power density and in the last decade it was said [3] that the limit would be the thermal management predicting an ultimate 10 W/µm^2 as figure of merit.

II. Power HBT technology : status

In a general use, the SHBT technology uses an integrated emitter ballast resistance to prevent a thermal runaway. This choice is more efficient than the use of an external base ballast resistance associated to a parallel MIM capacitor. Thus, the risk of hot spot in the emitter finger is reduced. In order to decrease the thermal resistance of the device, a thick gold layer is put down each emitter finger, improving the cooling and the temperature uniformity through the transistor. Note that the emitter inductance could be decreased by an appropriate design of this radiator.
The collector is designed to sustain a BVcb0 value close to 28V corresponding to a BVce0 of 18V (Ib=1µ - β = 20). The maximum collector current density is near of 90 / 100 kA/cm^2 corresponding to the Kirk effect for which ft is dropping.

To obtain high power level, several elementary fingers have to be combined by the way of an adequate topology depending of the frequency range of interest. Typically, the parallel topology is preferred for X and Ku Band applications, the fishbone topology being used for C bands. Note that this former method of combination allow a high level of integration in term of W / mm^2 (GaAs substrate).
With these characteristics, RF results in the range of 4 W/mm have been demonstrated on multi-fingers devices (1.2W / 55% PAE at 10GHz or 4W / 60% PAE at 3 GHz, both in CW mode).

New developments are underway based on single and double HBTs technologies to increase power level available by chip in shifting the frequency limit towards 40 GHz, both keeping constant the use of GaAs as mother substrate. Work aiming to decrease the thermal heating in CW or pulsed mode is the motor of these researches and defines the maximum limit in power density. Different approaches have been done or suggested in the past. One of the most famous result was published in [4]. Recently, in the scope of the European project named APOS [5], a significant progress has been obtained by the way of flip- chip mounting process. To fulfil these objectives, the growth of thick power bumps has been made directly on top the transistor (emitter fingers). Thus, a 30% improvement of the Rth have been got keeping safe the reliability level of the HBT technology in use. First successful demonstrations have been made on elementary devices and MMIC (1W @ 11 GHz - CW).

III. Path of successes for HBTs: Mastering of microwave and thermal fields.

A. Power density

The increasing of the power density is dependent of the product Ec x Jc max where Ec is the maximum electric field before breakdown and Jc the maximum collector current before Kirk effect. Notice that these parameters are related to the doping used in the collector, the thickness being of importance for the breakdown voltage and the cut-off frequency ft.
An optimum has to be found depending on the applications. In table 1, we give the numerical values used for two distinct applications.

The maximum bias voltage (collector) could go beyond the BVce0 / 2 limit without sudden burning of the device. This assessment is valid for base and emitter common configurations. To explain this fact, a waveform analysis is done on an overdriven transistor corresponding to a high power / high efficiency mode of operation. It could be observed that when the collector voltage reach is maximum value then the base emitter diode is off. In that case the BVcb0 instead of BVce0 gives the maximum voltage limit, no current amplification (β factor) couldn't occur. In figure 1, the RF performances of a 8 fingers of 2 x $30\mu m^2$ are represented for a collector bias ranging from 9 to 12.5V for which BVce0 is close to 18V at Ib=1µA.

The topology of the transistors is of prime interest to improve the power density. First challenge is about the maximum sizing of the finger length. Today, typical emitter lengths are ranging between 20 and 40 µm for applications up to Ku band, 70µm up to C band. In comparison to FET technologies, these figures are much lower and explain there is no significant difference in the output power between a 1W/mm HFET or PHEMT transistor and a 3.5 W/mm HBT transistor. To understand and go beyond this limitation, a distributed model of a single finger has to be designed. The influence of the base resistance distributed along each base stripe is the key factor. In decreasing this one (metal thickness, topologies), multi-fingers power HBT with finger length rising up to 100µm is possible up to X band.
The second alternative to increase the power density is to design a new topology of elementary finger. Standard cell use two base stripes from each side of one emitter finger. The other possibility is to have only one central base stripe with two emitters. Both topologies used the same U shape collector combiner. This former solution addresses the last request to minimise the distributed effect

along the base stripe. Furthermore, the output power from this bi-cell topology is doubled in comparison to a classical one with a slight impact on the overall dimensions of the chip (figure 2).
The last field of interest affects the topology used to combine fingers between them. Two topologies are useful: parallel and distributed (also named fishbone). First one is suitable for applications ranging up to Ku band, the second one being limited to C band. Reason explaining this difference is the associated RF gain 1.5 dB higher in the parallel topology. An other important limitation is the decreasing of the RF power gain versus the number of fingers. For X-Band applications, it is more convenient to limit this figure at 10 fingers in order to satisfy a high PAE. As already pointed out with the use of very long emitter finger, the distributed effect is the key point to solve. About the fishbone topology, a recent paper [6] propose a new input combiner to decrease this effect, trying to minimise the input inductance (Lb) connecting each finger to the main feeder. Concerning the parallel topology, it is critic to obtain the same improvement on the emitter inductance (Le) which connects each finger by the way of a heat spreader. A very promising method would be to integrate a micro via hole under each emitter pad. These improvements would allow keeping constant the RF power gain versus the number of fingers and so obtain 1.5 to 2 dB in adding.

B. DHBT Collector-up

More advanced improvements are coming from the DHBT Collector-up transistor. By mixing of the intrinsic advantages of this structure (high breakdown, high fmax) and the precedent study, we get the best power device competing the PHEMT up to 40 GHz. Nevertheless, special attention has to be paid to the design and fabrication of the base-collector transition region to suppress current blocking. Also, the electron recombination has to be minimised in the extrinsic base to satisfy a high current gain value.

C. Thermal management of high power HBTs

As already mentioned, the thermal management of power HBT is the key issue. Referring to the last part, a minimum factor 2 improvement on the thermal resistance (Rth) is awaited. In the case of pulsed operating mode, the transient behaviour of the thermal heating has to be also considered.
Power Flip-chip mounting is a first approach for which [4] a 30% improvement on Rth has been recorded. The transferred substrate technique proposed by Rodwell [7] et al is another good suggestion. However, all these solutions are complex in term of manufacturing and the impact on the yield is problematic. Thinning of the substrate down to few tens of micrometers is not easier for a manufacturing process using 4 or 6” wafer.

The increasing of the thickness of the thermal heat spreader (gold based) beyond 25µm put severe problems during the back end processing of the wafers. An advance thermal management has been developed using materials with high thermal diffusive and conductivity properties to stabilise and limit the thermal heating. These solutions are pertinent and efficient for a pulsed mode of operation and could be extend easily to a CW mode. A factor 2 improvement on the Rth has been measured on different configurations of power HBT. For a transient mode, the temperature is stabilised and the drift cancelled in a few µs. First concept developed in these work are based on the use of thick copper or diamond materials on top the emitter finger. The thin gold heat spreader act as attachment with the “thermal sponge”.

IV. Conclusions

After a short review of the applications address by high power HBT technologies, a complete and exhaustive description of some improvements has been done. As often stressed, the HBT

technology will be limited by thermal heating and reliability level. Using some improvements described above, a 50% increase in performances could be expected. The power density would reach 8 to 10 W/mm form L to S band to drop to 6W/mm in Ku band. More advanced structure (DHBT Cup) will push away these limits near 40 GHz to address power needs. Future is bright for power HBTs.

Max. operating frequency	**Up to 4 GHz**	**Up to 18 GHz**
1. Collector doping	4 to 6 10^{15}	1 to 2 10^{16}
Collector thickness (µm)	2.8 to 3.2	0.9 to 1.2
BVcb0 (V)	60 to 65	28 to 32
BVce0 (V) – Ib=1µA	34 to 37	16 to 18
Fmax (1W device – Vce=BVce0 /2)	40 GHz	18 GHz

Table 1 : DC and RF data on two high power HBT technologies.

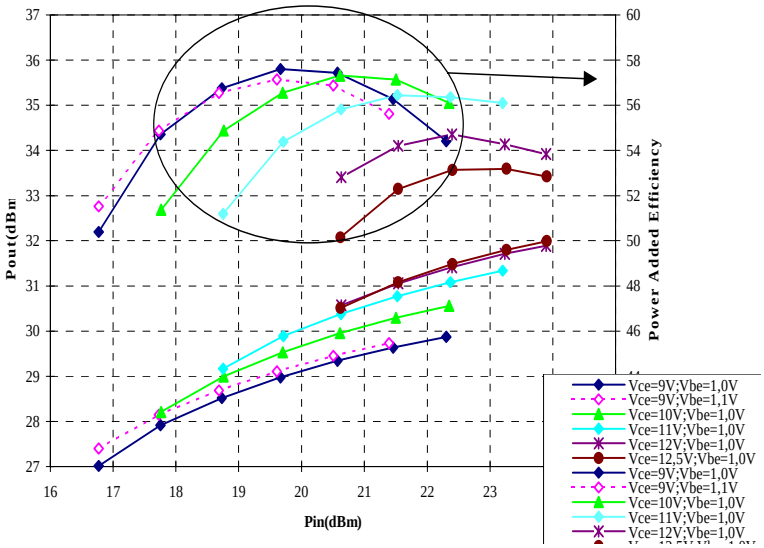
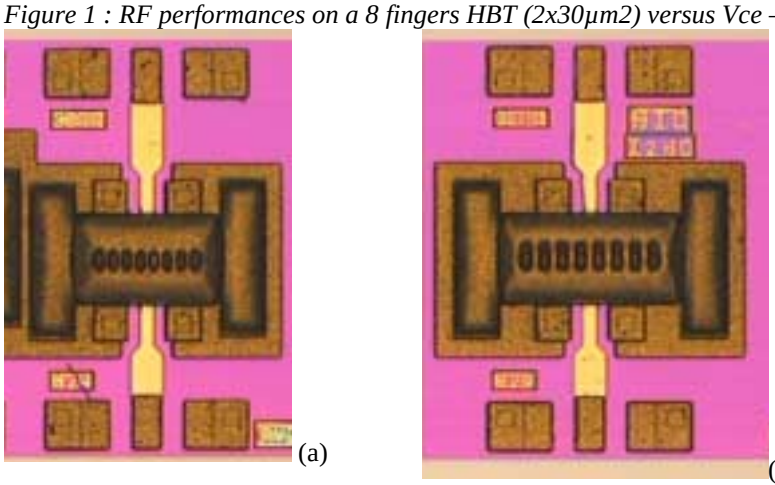


Figure 1 : RF performances on a 8 fingers HBT (2x30µm2) versus Vce – BVce0 = 18V/Ib=1µA.



(a) (b)

Figure 2 : Comparison between a 1W (a) and a 2 W power transistor (b) based on bi-cell topology.

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