

RF POWER PERFORMANCE OF PASSIVATED ALGAN/GAN HFETS GROWN ON SiC AND SAPPHIRE

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ABSTRACT

We have analysed the impact of SiN surface passivation on the performance of undoped (piezo) AlGaN/GaN HFETs grown on SiC and sapphire. Though there is little change after passivation in carrier concentration and mobility as evidenced by Hall measurements the RF power performance is significantly improved leading to state of the art power densities of up to 6.5 Watt/mm at 10GHz and absolute power of 6.6 Watt cw for a 1.2mm piezo device on SiC substrate.

INTRODUCTION

GaN/AlGaN HFETs have attracted considerable interest in the last few years for power applications at high frequencies. The considerable effort stems from the unique material properties of the III-Nitride semiconductors leading to high breakdown fields in conjunction with good electron transport properties. The GaN/AlGaN HFET technology offers especially large potential to surpass existing device limitations in RF output power, operation voltage and operation temperature at frequencies up to X-band and even above. Indeed impressive high frequency results have been reported recently for GaN/AlGaN HFETs with record power densities of up to 9.8 Watt/mm measured at 8 GHz by Wu et al (1). In this paper we discuss our recent results on passivated piezo GaN/AlGaN HFETs grown on SI SiC and sapphire by MOCVD. It is shown that the so-called "current compression" effect could be significantly reduced for both device structures using a thin SiN passivation layer.

TECHNOLOGY

The wafers were grown by MOVPE using a Thomas Swan Close Coupled Showerhead reactor. Trimethyl Gallium and Trimethyl Aluminium were used as the group III precursors and the growth was monitored in real time by spectral reflectometry (300-750nm).

Two piezo wafers were grown with nominally the same vertical structure: one wafer on semi-insulating SiC substrate (wafer A) and one wafer on sapphire substrate (wafer B). A typical HFET structure consists of a nucleation layer, a 1 μm thick GaN buffer layer and an undoped 28nm thick AlGaN layer with Al content of 24-26%.

The device fabrication was performed using mesa isolation with BCl_3/Ar gas, ohmic metallisation with Ti/Al/Ni/Au annealed at 900°C for 30 seconds and formation of a T-shaped e-beam gate (Ti/Au) with 0.45 μm gate-length. Then a 200nm thick PECVD SiN deposition at 300°C followed. CF_4/O_2 -RIE was used to open contact holes in the SiN layer. Finally Au air-bridges with 2.5 μm thickness were fabricated to connect the source pads of multi-finger devices. TLM analysis shows for both wafers contact resistances of 0.5 $\Omega\text{m} \times \text{mm}$ and sheet resistances between 500 and 600 Ω/sq .

DC PERFORMANCE

The Hall sheet concentrations and mobilities received from wafer A and B are nearly identical and within the experimental uncertainty unaffected by SiN passivation. This behaviour is consistent with recently published results [2]. The corresponding values for both wafers are:

- Wafer A: $n_s=1.1 \times 10^{13}/\text{cm}^2$, mobility of $1100 \text{cm}^2/\text{Vs}$
- Wafer B: $n_s=1.0 \times 10^{13}/\text{cm}^2$, mobility of $1170 \text{cm}^2/\text{Vs}$.

The I-V characteristics, however, reveal a significantly lower I_{dss} for the devices grown on sapphire compared to SiC. The passivated (unpassivated) drain currents at $V_{gs}=0\text{V}$ for small area devices on wafer B correspond to $680 \text{mA}/\text{mm}$ ($630 \text{mA}/\text{mm}$) whereas the same devices on wafer A exhibit values of 1250mA (1150mA). Also the maximum transconductance of unpassivated devices on wafer A are about 30% higher compared to the corresponding devices on wafer B ($220 \text{mS}/\text{mm}$ compared to $170 \text{mS}/\text{mm}$). After passivation a slight increase of about 10% in g_m is observed which correspond to recent results on doped AlGaIn/GaN HFETs [2,3]. The relative large difference in I_{dss} could be partly explained by the better heatspreading and heat removal for devices on SiC. Indeed, pulsed I-V measurements performed on devices of wafer B show an increase of I_{dss} of up to $880 \text{mA}/\text{mm}$.

The observed increase of I_{dss} in our experiments after SiN deposition could obviously not be explained by an increase of n_s . Also we found that the threshold voltage didn't change significantly ($<0.1 \text{Volt}$) after passivation in good agreement with the constant n_s from the Hall measurements. However, the results could be understood in terms of a change of the effective gate-length due to passivation. Assuming charged surface states in the gate-drain region of the AlGaIn/GaN HFET without SiN passivation an enhancement of the lateral gate-drain depletion region will occur, resulting in a longer effective gate-length, hence lower maximum transconductance and saturation current. The SiN layer compensate charged surface states, leading to a reduced effective gate length as discussed by Lee et al (2). A comparison of the small signal equivalent circuit parameters of unpassivated and passivated devices carried out by Lee et al (3) reveals a decrease of the transit time for passivated devices consistent with the above speculation.

RF POWER PERFORMANCE

RF power measurements have been performed at 2GHz and 10GHz. At 2GHz a load-pull setup with ATN tuners have been used. It should be mentioned that for this setup the load conditions could not be fully optimized for the smaller devices due to the setup limits and larger devices could not be driven in compression due to a limited power source at 2GHz. At 10GHz the measurement system is based on a Wiltron Model 360B Vector Network Analyser with a Model 3636A test set. For load tuning an active load tuner is applied with up to 20 Watt power handling in the frequency range of 8GHz to 18GHz. As reference, a part of our devices have been measured at Agilent, Santa Clara. All power results presented have been achieved by biasing the devices at class AB. Due to self-biasing the current typically increases during a power measurement.

The impact of SiN passivation on the RF power performance have been studied first at 2GHz. HFET devices with $2 \times 100 \mu\text{m}$ gate width have been selected for this comparison. Fig.1 depicts P_{out} , gain and PAE versus P_{in} for a passivated and an unpassivated device of wafer B (sapphire) at $V_{ds}=25 \text{ Volt}$ and $V_{gs}=-3.8 \text{ Volt}$. The unpassivated device delivers $1.7 \text{W}/\text{mm}$ saturated output power density and the passivated device shows an improved power density of $3.1 \text{Watt}/\text{mm}$. The corresponding maximum PAE increases from 41% before passivation to 55% after passivation. From the load impedance Z_L , which was the same for passivated and unpassivated devices one can estimate the current and the voltage swing. We obtain $490 \text{mA}/\text{mm}$ and $660 \text{A}/\text{mm}$ for the unpassivated and passivated devices, respectively, demonstrating that the reduced output power for unpassivated devices is due to a limited RF current drive. In contrast, for passivated devices the calculated current swing is very close to I_{dss} (see above) corresponding to a large reduction of the current compression effect.

Higher absolute output powers and power densities have been achieved at larger drain bias. At $V_{ds}=35 \text{V}$ a P_{out} of 28.7dBm corresponding to $3.7 \text{Watt}/\text{mm}$ with an associated gain of 11dB and a PAE of 40% is obtained.

As expected we observe only a slight decrease of the linear power gain which is probably due to the increased C_{gd} after passivation (see Fig.1). The observed large increase of power densities after passivation have been seen on all measured devices of wafer B (22 devices measured).

Fig. 2 shows the corresponding comparison of unpassivated and passivated $2 \times 100 \mu\text{m}$ devices on wafer A (SiC). Similar as for the devices on wafer B a strong increase in P_{out} and PAE is observed after passivation. At the bias point of $V_{ds}=25\text{V}$ and $V_{gs}=-4.5\text{V}$ the RF power is increased from 24.8dBm to 29.1dBm and the PAE increases from 35% to 59%. The highest output power on the passivated $2 \times 100 \mu\text{m}$ devices have been measured at $V_{ds}=40\text{V}$ with $P_{out}=30.9\text{dBm}$ (6.1Watt/mm) and $\text{PAE}=42\%$.

Load-pull measurements at 10GHz have been performed on passivated devices on wafer A (SiC). Fig. 3 depicts the output power, PAE and gain of a $4 \times 50 \mu\text{m}$ device biased at $V_{ds}=45\text{V}$. We achieve a power density of 6.5Watt/mm with an associated PAE of 42%. The highest absolute cw output power have been achieved on a 1.2mm device ($8 \times 150 \mu\text{m}$) at $V_{ds}=37\text{V}$ (Fig.4) with $P_{out}=6.6\text{Watt}$ and a corresponding PAE of 46%.

CONCLUSION

The impact of SiN passivation on (piezo) AlGaIn/GaN HFET devices grown on SiC and on sapphire substrate have been reported. We demonstrate that the RF power performance is dramatically enhanced by deposition of a thin SiN film for devices on sapphire as well as on SiC. Maximum output power levels of 6.6Watt cw and 6.5Watt/mm at 10GHz have been achieved. We observe little change after passivation in carrier concentration and mobility as evidenced by Hall measurements. Our results are consistent with the assumption that during RF drive the surface of the unpassivated device (e.g. between gate and drain) is negatively charged depleting the channel and thus limiting the RF current amplitude.

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Fig.1: Power sweep at 2GHz before and after SiN passivation (Wafer B, sapphire substrate)

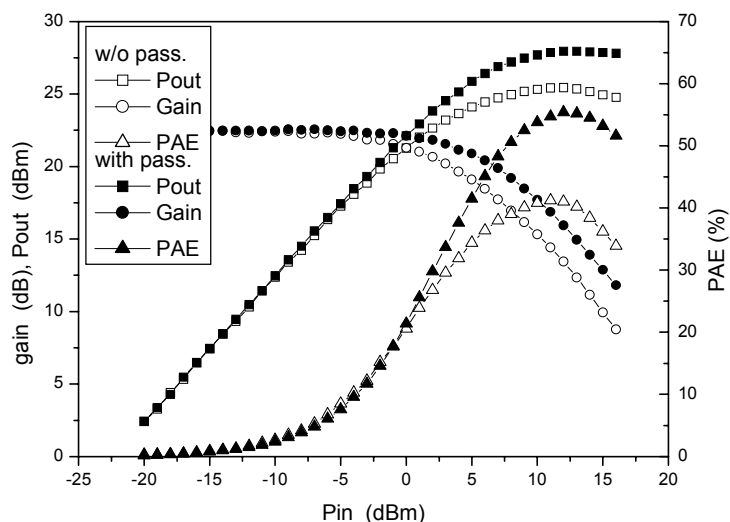


Fig.2: Power sweep at 2GHz before and after SiN passivation (Wafer A, SiC substrate, 2x100 μ m, Vds=25Volt)

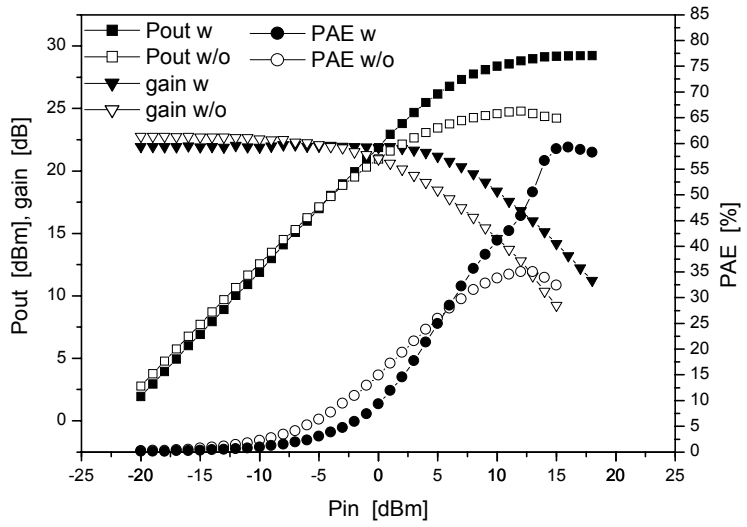


Fig.3: Power sweep at 10GHz after SiN passivation (Wafer A, SiC substrate, 4x50 μ m, Vds=45Volt)

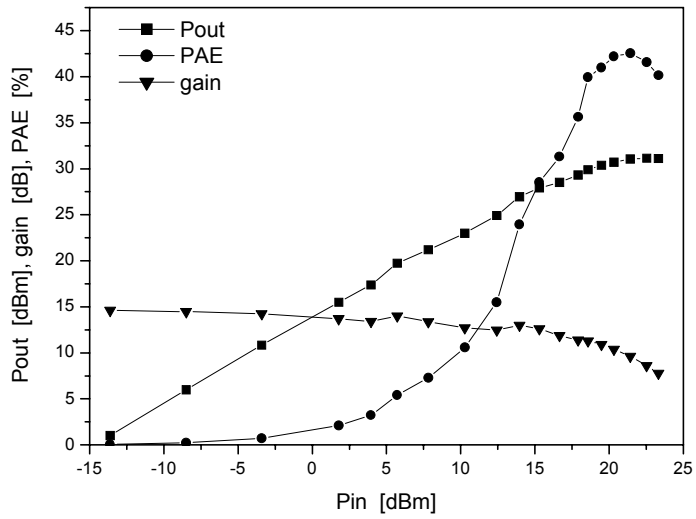


Fig.4: Power sweep at 10GHz after SiN passivation (Wafer A, SiC substrate, 8x125 μ m, Vds=37Volt)

