# AlGaN/GaN HFET'S

by

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## ABSTRACT

The strong spontaneous and piezoelectric polarizations in pseudomorphic AlGaN/GaN on SiC substrates are used to induce 2DEG sheet density of > 1 x $10^{13}$/cm$^2$ with mobility up to 1,700 cm$^2$/vs. The processing sequence and HEMT electrode layout are presented. The output power and power-added efficiency in the 8-10 GHz frequency range are shown for CW bias conditions and optimum tuning in class B operation. Single-gate, center-fed 100 µm periphery devices gave 11.2 W/mm at 32% power-added efficiency; two-gate, 200 µm periphery devices with 50 µm pitch gave 8.7 W/mm at 48% power-added efficiency, and 12-gate, 1.5 mm periphery devices with 50 µm pitch gave 6.7 W/mm at 42% power-added efficiency. For comparison, the latter gave 9.4 W/mm at 43% power-added efficiency in low duty cycle pulsed operation . The key limitation for CW power performance is self-heating, which raises the knee voltage by $(T/300)^{1.8}$ for T channel temperature in °K.

## INTRODUCTION

It has been a hope that ultra-high microwave power amplification would be possible using semiconductor heterojunction devices. The requirement would be for much higher operating voltage and current, compared with present semiconductor devices, as well as effective heat removal through the device substrate. In addition, the frequency response should also be made comparable with present devices. AlGaN/GaN HFET's on SiC substrates have now begun to show all these attributes. The GaN channel has 7.5 times the breakdown field of GaAs, due to its 3.4 eV bandgap. Its average electron transit velocity is 1.3 x $10^7$ cm/s, comparable with that of GaAs MESFET's, but with the possibility of reaching 2.4 x $10^7$ cm/s, which is comparable to that of InP HEMT's. The 2DEG in this GaN HEMT is in the 1.0-1.2 x $10^{13}$/cm$^2$ level, yielding $I_{dss}$ value above 1 A/mm. The semi-insulating SiC substrate has a thermal conductivity of ≥ 3 W/cm-$^o$K, which is ~ 7 times that of semi-insulating GaAs. For comparable load resistances, these nitride HEMT's, with scaled up periphery values, will be able to supply ~ 50 times as much power as GaAs power HEMT's. The layered material can be grown by OMVPE or MBE, and needs no doping, due to a combined strong spontaneous electrical polarization and a strong piezoelectric polarization.

## TECHNICAL BACKGROUND

Because of its non-centrosymmetric Wurtzite crystal geometry and its atomic charges, there is a strong spontaneous polarization in both AlN and GaN (1), with the former having the largest amount. In addition, when a pseudomorphic AlGaN layer, less than critical thickness, is grown on GaN, it has a strong piezoelectric polarization (1). Growth of a pseudomorphic $Al_xGa_{1-x}N$ barrier on GaN thus yields a positive polarization charge of 5.5 x $10^{13}$/cm$^2$ times electronic charge times the fraction x at the heterojunction (2). The dependence on x is bowed, yielding 6.2 x $10^{13}$/cm$^2$ times the electron charge for AlN/GaN. In order to be pseudomorphic, the $Al_xGa_{1-x}N$ thickness must be less than 400 Å for x = .30, and less then 50 Å for x = 1.0. The surface potential of the $Al_xGa_{1-x}N$ is nearly fixed at the Ni Schottky barrier value of (.9 + 1.9 x) V which allows the heterojunction polarization charge to induce a 2DEG in the GaN buffer/channel. Except for surface depletion, and depletion around charged dislocations, the 2DEG charge density can nearly reach the polarization charge density at the heterojunction, since the electric field under the 2DEG is small. The mobility of the electrons in the 2DEG, for 1 – 1.2 x $10^{13}/cm^2$ electrons, has experimentally reached 1,700 $cm^2/V$-s. The polar optical phonon limit to this mobility is 2,500 $cm^2/V$-s (3), and the experimental mobility is lower due to the interface/alloy scattering, as well as due to the charged dislocations. The latter are ~ 5 x $10^8/cm^2$ for optimized growth on SiC, and ~ 2 x $10^9/cm^2$ for optimized growth on Sapphire, and each dislocation traps ~2,000 electrons in thermal equilibrium The electron mobility reduction (4) in bulk GaN was shown to be more severe for low donor densities, and for very low donor densities depletes all of the electrons. This allows undoped GaN buffer layers to have bulk resistivities > $10^8$ Ω-cm. The 2DEG sheet resistance ranges from 300-500 Ω/square, and experimentally rises with temperature as $(T/300)^{1.8}$. Schottky gates using Ni on $Al_{.3}Ga_{.7}N$ are able to withstand the high electric field of ~ 3.5 M V/cm encountered at channel punch off. At 300 °K temperature the thermally-assisted tunnel current is simulated (5) to be ~ 30 nA/mm for .25 μm gates. Experimentally the leakage current is ~ 50 nA/mm for this gate length at room temperature. The temperature rise in the GaN channel for self-heating has been simulated in 3 dimensions, using a thermal conductivity of 3.3 (300/T) $W/cm^{-}°K$ for the temperature in Kelvins. It yields ~ 160° temperature rise for 10 W/mm heat dissipation, and for many parallel 125 μm channels with 50 μm separations between channels. This temperature raises the sheet resistance and the knee voltage by a factor of nearly 2.2, lowering the drain efficiency.

Initially these HEMT's had a substantial current slump, or DC to RF dispersion, when operated at high drain bias. This was caused by electrons reaching empty surface states by tunneling out of the gate and by being excited out of the channel by high electric fields. In order to stabilize the surface charge, it was discovered (6) that $Si_3N_4$ deposited by PECVD on the AlGaN surface strongly alleviated this current-clump condition.

## EXPERIMENTAL RESULTS

The processing sequence includes: alignment mark formation, mesa isolation, ohmic contact formation, Schottky gate formation, first level metal deposition, $Si_3N_4$ passivation, and air bridge formation. Mesa isolation is made using $Cl_2$ ECR etch of 2,000 Å. Ohmic contacts use 200 Å Ti, 1000 Å Al, 450 Å Ti, and 550 Å Au annealed at 800° for 30-60 seconds. Mushroom-cross section gates are formed with electron beam tri-level resist and 200 Å Ni and 3,600 Å Au. The first level metal has 250 Å Ti, 3,500 Å Au, and 100 Å Ti. The PECVD deposition of $Si_3N_4$ is 3,200 Å thick and is deposited at 300°C with ~ 50 W exitation at 50 KHz. Finally the air bridge has 250 Å Ti, 750 Å Au, followed by 1 μm Au plating.

The small signal frequency response yielded 74 GHz extrinsic $f_t$ for .15 μm footprint, and 19 GHz extrinsic $f_t$ for .75 μm footprint. When adjusted to give intrinsic $f_t$, thus yielded on average electron transit velocity of 1.3 x $10^7$ cm/s. This is much lower than the 2.85 x $10^7$ cm/s peak velocity calculated by Monte Carlo calculations (7). More research is required to understand this condition. The effective gate length was the gate footprint plus 2 d where d is the $Al_{.3}Ga_{.7}GaN$ barrier thickness of ~ 250 Å. These same .15 μm and .75 μm gate lengths yielded drain-source breakdown voltages of 35 V and 140 V, respectively. A figure of merit can be determined from these results, with the intrinsic $f_t$ depending on the reciprocal of the effective gate length, and the drain-source breakdown voltage depending directly on the effective gate length. This figure of merit is:

$$F.O.M = P_A f_{10}^2 Z_L = 1.2 \times 10^{23}\ WHz^2\,\Omega. \qquad (1)$$

Where $P_A$ is the maximum class A power, $f_{10}$ is the maximum frequency yielding 10 db saturated power gain, and $Z_L$ is the load resistance.This F.O.M. is ~ 50 times that for GaAs MESFET's, and 1.8 times that for SiC MESFET's. These latter two technologies are limited to somewhat lower frequency operations.

When properly passivated with $Si_3N_4$, $Al_{.3}Ga_{.7}N$/GaN HEMT's with .3 µm gate footprints on SiC substrates were characterized CW in class B operation in the 8-10 GHz range. A single- gate, center-fed HEMT with 100 µm periphery yielded normalized power density of 11.2 W/mm at 32% power-added efficiency at 45 V drain-source bias. It had ~ 500 Ω load resistance, and had 24 W/mm heat dissipation, with~ 10°/W/mm thermal resistance. With two, parallel gates, 50 µm apart in a 200 µm periphery, the HEMT yields normalized power density of 8.7 W/mm at 48% power-added efficiency at 40 V drain-source bias. It had a ~ 240 Ω load resistance, and had 9.5 W/mm heat dissipation with ~ 13°/W/mm thermal resistance. When 12 gates, 125 µm wide, were included in the layout, all in parallel with 50 µm separation, the 1.5 mm periphery device yielded 6.7 W/mm power density at 40% power-added efficiency at 32 V drain-source bias. It had ~ 27 Ω load resistance, and had 10 W/mm heat dissipation with ~ 16°/W/mm thermal resistance. In all cases these devices had much higher power-added efficiency, being 63%, 72%, and 50% respectively in the 13-15 V drain-source bias range. The high power-added efficiency for the 200 µm periphery device was due to the fact that the Maury$^{TM}$ automatic turner in the output could impedance-match this device better than the others. As the drain voltage was raised on all of these devices, the self heating substantially raised the instantaneous minimum voltage during the microwave voltage swing. This could be seen using our method of displaying the dynamic load line as the bias voltage was raised, while drive power was increased to the point of microwave power saturation. For comparison, pulsed operation at .01 duty cycle and 500 nsec pulse length was done to reduce the self-heating in the 1.5 mm periphery HEMT, and yielded 9.4 W/mm into a 35 Ω load resistance, at 40 V drain-source bias, at 43% power-added efficiency. This test was limited, by the available drive power, to the 2 db gain-compression point, while the CW tests were made up to 4-6 db gain compressions.

These devices were given preliminary noise tests. With .3 µm gate footprint, a 1.3 db microwave noise figure was gotten at 10 GHz. This value is comparable with that of GaAs HEMT's with the same gate length and at the same frequency. Although not yet fully optimized, the average $1/f$ noise varied over 8 db, depending on the materials structure and processing procedure. With $Si_3N_4$ passivation and a potential barrier of AlN below the channel, the lowest average $1/f$ noise was achieved.

## CONCLUSION

AlGaN/GaN polarization-induced HEMT's on SiC substrates have yielded new record power performance in class B operation in the 8-10 GHz range. CW operation of 1.5 mm periphery HEMT's in class B operation yields nearly 7 W/mm, and should exceed 10 W/mm with design improvements. These devices will be the choice of systems engineers, needing up to 100 W at frequencies up to 10 GHz

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